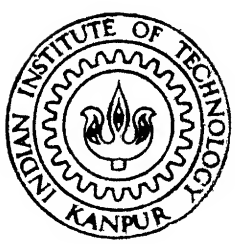
Three-Phase Instantaneous Reactive and Harmonic Power Compensation Using Multi-level Inverters at Constant Switching Frequency

by

Brajendra Kumar Bhujabal



DEPARTMENT OF ELECTRICAL ENGINEERING

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Brajendra Kumar Bhujabal

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CERTIFICATE

This is to certify that the work contained in the thesis entitled **"Three Phase Instantaneous Reactive and Harmonic Power Compensation Using Multi-level Inverters at Constant Switching Frequency"** by *Mr. Brajendra Kumar Bhujabal*, has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

4/5/98

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Dedicated To

My

Ullas Bhai

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ABSTRACT

The thesis work involves instantaneous reactive and harmonic power compensation of a three-phase system. A typical controlled rectifier load is considered to create harmonics and phase displacement for the source current. Using the concept of instantaneous power the compensator system performs well both in steady state and transient state as well. The main intention is to operate the voltage source inverter at Constant Switching Frequency with relatively a low value of inductor. Because of a small inductance, the response of compensator system becomes faster. Due to constant switching frequency technique the system becomes more compact and reduces switching losses and device stresses.

The voltage source inverters studied, include two-level, three-level and five-level inverters. Higher level inverters increase the complexity and need voltage control even for a lossless system. A three-phase three-level inverters, consisting of three wye-connected single-phase inverters, is studied for the compensator system. It has been found that this configuration needs no additional voltage control aspect for a lossless system. This three-level inverter is operated at constant switching frequency to obtain instantaneous reactive and harmonic power compensation. System losses are included and the capacitor voltages are held constant with an outer voltage control loop. The study reveals that the compensator employing wye-connected three-phase three level inverter provides independent voltage and current control capability with all the advantages associated with constant switching frequency.

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NOMENCLATURE

e_a, e_b, e_c	Instantaneous system phase voltages.
i_{sa}, i_{sb}, i_{sc}	Instantaneous system phase currents.
i_{sa}^*, i_{sb}^*, i_{sc}^*	Instantaneous system phase currents under ideal compensation.
i_a, i_b, i_c	Instantaneous load phase currents.
i_{ca}^*, i_{cb}^*, i_{cc}^*	Instantaneous compensator phase reference currents.
i_{cma}, i_{cmb}, i_{cmc}	Instantaneous compensator phase output currents.
E_{an}, E_{bn}, E_{cn}	Instantaneous compensator phase output voltages.
L_c	Interfacing inductance between inverter and system.
R_c	Resistance representing system losses and internal resistance of inductor.
A, B, C	Switching signals from current controller for inverter phases.
p, q	Instantaneous active and reactive power.
$\tilde{p}$, $\bar{p}$	Alternating (ac) and Average (dc) Component of instantaneous active power.
$\tilde{q}$, $\bar{q}$	Alternating(ac) and Average(dc.) Component of instantaneous reactive power.
k_{a1}, k_{a2}, ...	Switching devices of phase-a of the inverter.
k_{b1}, k_{b2}, ...	Switching devices of phase-b of the inverter.
k_{c1}, k_{c2}, ...	Switching devices of phase-c of the inverter.
i_{trg}	Instantaneous value of the triangular wave.
δ	Magnitude of the triangular wave.
f_c	Frequency of the triangular wave.
f_{sw}	Switching frequency of the devices.

Chapter 1

INTRODUCTION

1.1 Introduction

It is well established practice to use reactive power compensation to control the magnitude of the voltage at a particular busbar in electric power system or to improve the power factor of the system. In the past, synchronous condensers, mechanically switched capacitors and inductors were used to control the vars. Due to the advent of switching devices like thyristors, in late 1960s, thyristor controlled reactor (TCR) together with fixed capacitors or switched capacitors (TSC) have been used to inject or absorb reactive power. These schemes involve bulky and expensive elements. Advanced static VAR generator was presented, but required additional filters to compensate the harmonics [5]. The filters add to the impedance of the system resulting in slower response. An Advanced Static VAR Compensator (ASVC) was presented, employing the popular three level VSI topology to compensate the reactive power and the inverter was operated in selective harmonic elimination modulation (SHEM) technique to minimise the harmonics [6]. However, the compensator using instantaneous reactive power theory gives excellent compensation characteristics [1], [2]. Unlike the conventional reactive power compensators like SVC, which can eliminate only the fundamental reactive power in steady state, the Compensator System based on instantaneous reactive power concept eliminates the fundamental reactive power and current harmonics in transient state as well as in steady state [2].

1.2 Literature Review

Akagi [1] presented an instantaneous reactive power compensator discussing the conceptual theory of instantaneous reactive power. Balanced loads were taken into consideration and the compensation was obtained with a two-level inverter. The compensator compensates the fundamental reactive power and a part of the harmonic power. Experimental results for a diode bridge load and a cyclo-converter load were illustrated. Alternating component of active power which also contributes to harmonics, was not compensated.

Watanabe [2] presented the concepts of instantaneous active and reactive powers. It clearly explains all the components of instantaneous active and reactive powers from compensation point of view. It also brings out that the instantaneous alternating active power is to be compensated to eliminate harmonics.Since the sum of this component of power contributed by all the three phases is not zero instantaneously, it contributes to energy exchange and hence leads to dc voltage deviation of the inverter.

Akagi [3] utilized multiple voltage source inverters for instantaneous power compensation. It used the two level configuration of the inverter and compensated the harmonics fully by compensating alternating component of active power. To separate this component, it utilised a butterworth filter which has its own delay time. The multiple source inverter was used to suppress the harmonics caused by the switching operation without increasing the switching frequency. It makes the system complicated. Unbalanced loads were, however, not studied for the compensator system.

Kazerani [4] presented a novel current waveshaping technique for a dc-dc boost converter at constant switching frequencies. It illustrated the experimental results for the boost converter. This was not explored for active power filter.

Ekanayake [6] presented a Static Var Compensator using a three-level inverter. It is based on the conventional reactive power concepts. Harmonics are minimized by selective harmonic elimination modulation (SHEM) technique and experimental results were shown. Hence, it could not compensate the harmonics fully. It shows the experimental results of a laboratory model and the determines the speed of response of the scheme.

Nabae [7] has presented the neutral-point-clamped (NPC) three-level inverter. The inverter was operated in PWM technique to make the output voltage of the inverter close to sinusoidal. The three-level operations were clearly described and experimental results were also illustrated. Hochgraf [8] presented a five-level inverter used as static compensator for a high voltage (13.8 kV) distribution system. It finds out the component ratings of the multi-level inverter. It also illustrated the simulation results for the compensator.

Aburto [9] presented an active power filter with the NPC three-level inverter using the instantaneous reactive power concept. It presented the principles of operation and design criteria for both power and control circuits. It implemented space vector modulation technique for controlling the current. Simulation results were presented for the system. It has an outer voltage control loop for taking care of the active losses in the inverter. Again, it included the voltage control aspects in the current controller action, thus deteriorating the response of current controller. This is because, the NPC Inverter configuration when used to compensate only reactive power of a loss-less system, shows steady increase in dc input voltages of the inverter. Thus this inverter configuration makes the system less stable.

1.3 Thesis outline

The Reactive and Harmonic Power Compensator simulated and presented in this thesis is based on the instantaneous reactive power concept for obtaining the reference currents for the inverters so as to eliminate the fundamental reactive power and current harmonics caused by the load. The source, assumed to be balanced, is having a maximum line to line voltage of 400 V. A typical controlled rectifier load is considered causing harmonics in the source currents. The controlled rectifier has a delay angle to create phase displacement of the source currents. The harmonics and the displacement factor are then improved by compensating the reactive and harmonic Powers instantaneously. The compensator system consists of multi-level inverters operating at constant switching frequency. Three-phase three-level inverter consisting of Wye-connected three single-phase inverters operating at constant switching frequency is also used as a compensator providing fast response, better voltage and current control capability when compared with the schemes reported in the literature.

The compensator system finds out the reference currents that could compensate the reactive power and eliminate harmonics, and then feeds the currents to the system by using voltage source inverter (VSI). This needs a reference current generator, a current controller, and a three-phase inverter. The reference current generator gives the instantaneous values of the reference currents and the current controller changes the switching conditions of the inverter so as to make the inverter current, that is fed to the system, follow the reference currents. Due to the system losses, the dc input voltage of the inverter deviates form the set value, thereby, requiring a voltage controller. These important features are illustrated in the block diagram shown in Fig. 1.1.

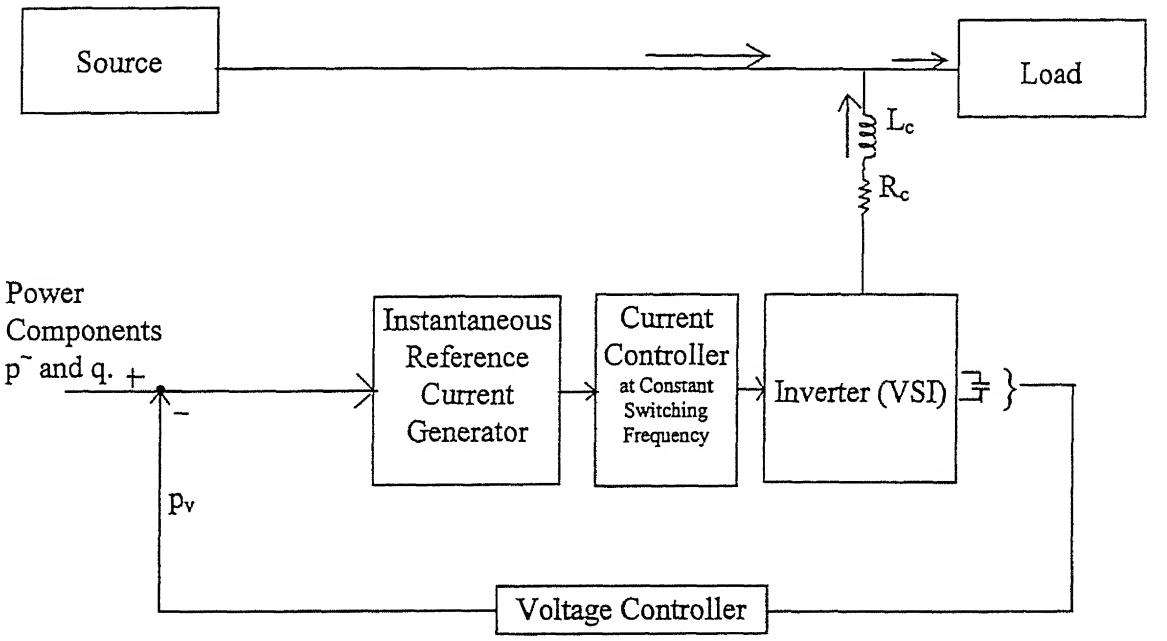

Fig. 1.1 : Compensator System showing important features.

The generation of reference currents is based on instantaneous active and reactive power concept. This makes the system to compensate reactive and harmonic powers, in transient as well as in steady state. Chapter 2 deals with the concept of instantaneous powers and the reference current generation. The current controller, used here, not only enables the inverter to operate at constant switching frequency but also allows to use a lower value of inductance L_c as shown if Fig. 1.1. Operating at constant switching frequency, the device losses and stresses are reduced. As a result, the size and rating of devices and the compensator system are also reduced. Lower value of

inductance L_c, makes the response faster and also reduces the size of the inductor. It has been found to be advantageous over the Bang-Bang Hysteresis type of current controllers. All types of configurations of inverters used for compensation, therefore, are operated at constant switching frequency. Chapter 3 explains the constant switching frequency technique using a three-level inverter for compensation. The results are compared with Bang-Bang Hysteresis control.

Compensation is obtained with three-phase voltage source inverters. Two-level, three-level and five-level inverters are used as three-phase voltage source inverters. All the inverters are operated at constant switching frequency. The two-level inverter, when used for compensation, fails to compensate under unbalanced load conditions. While compensation is obtained with these inverters, the system is assumed to be loss less, and hence voltage control loop is not used. It has been found that there is not much difference between the compensation characteristics, that are obtained with three level and five level inverters. Input capacitor voltages of these inverters are found to have steady increase/decrease even with loss-less system. All these are dealt in Chapter 4. It has also been found that, compensating only reactive power of the loss-less system also leads to steady increase/decrease of the capacitor voltages. This needs that voltage control aspect is to be included before switching the inverters. This affects the independent action of the current controller.

Chapter 5 deals with three-phase three-level inverter consisting of three Wye-connected single-phase inverters. The capacitor voltages of this inverter remain constant for the loss-less system. Thus, this configuration provides independent current control action and better current control capability. This does not need additional voltage control strategy for switching inverter devices. Hence it is relatively simpler to operate with no deviation of the average capacitor voltages. This three-level inverter operating at constant switching frequency is used to compensate reactive and harmonic powers of a system having losses. Any deviation in the capacitor voltages due to the losses, is controlled by the using outer voltage control loop. The voltage control loop uses a PI controller which compensates the effect of losses by modifying the magnitude of the reference currents.

Overall conclusions are drawn in Chapter 6 favoring the use of Wye connected three-phase three-level inverter which operate at constant switching frequency

for compensation as discussed in Chapter 5. Scope for further investigation is also included.

Chapter 2

FUNDAMENTALS OF INSTANTANEOUS REACTIVE POWER COMPENSATION

2.1 Introduction

The three-phase to two-phase transformation of voltages and currents makes it possible to separate active and reactive component of power from which the concepts of reactive power compensation can be studied not only in steady state but also in transient state. Using Park's power invariant transformation, the three-phase quantities (a,b,c) can be converted to '0-α-β' co-ordinate system. The zero sequence components are absent if we assume balanced system. The resulting co-ordinates are orthogonal to each other.

The active and reactive power each comprises of two components. One is the average or dc component and the other one is the alternating component. The instantaneous active and reactive powers are denoted as 'p' and 'q' respectively. The two components of p, are denoted as '$\tilde{p}$' and '$\bar{p}$' representing the alternating and average instantaneous active power respectively. Similarly '$\tilde{q}$' and '$\bar{q}$' represent the alternating and average instantaneous reactive powers.

The concept of instantaneous reactive power compensation involves that the source should supply only the instantaneous average active power while all other power components are supplied from the compensator as illustrated in Fig. 2.1.

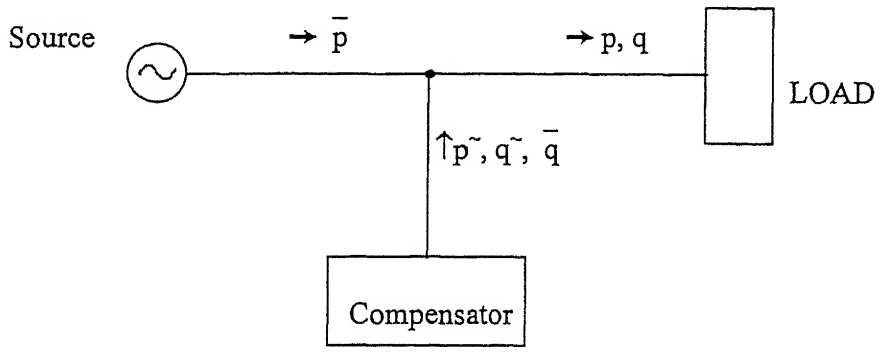

Fig. 2.1 : Block diagram of instantaneous reactive power compensator.

It is evident from Fig. 2.1 that it is required to separate $\tilde{p}$ and $\tilde{q}$ from p and q respectively. As $\tilde{p}$ and $\tilde{q}$ can not be directly obtained from the instantaneous voltages and currents sensed, some additional circuits are required to separate these alternating components. The technique of separating these alternating components $\tilde{p}$ and $\tilde{q}$ is explained in Sec. 2.3.

Section 2.4 reveals the effect of compensating the power components $\tilde{p}$, $\tilde{q}$ and $\bar{q}$ on the source currents. It also shows the transient response of the averaging performed over the instantaneous active and reactive powers. The source currents under ideal compensation when the compensator is assumed to supply the instantaneous values of reference currents, is shown in Section 2.4, revealing the excellent compensation characteristic of the "instantaneous reactive and harmonic power compensation".

2.2 Instantaneous Reactive Power Concept.

The instantaneous active and reactive powers are calculated by converting the three-phase quantities to equivalent two phase quantities by Park's power invariant transformation.

Converting the 3-ϕ instantaneous voltages to '0-α-β' co-ordinate system,

$$\begin{bmatrix} e_o \\ e_\alpha \\ e_\beta \end{bmatrix} = [k] * \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}. \tag{2.2.1}$$

where

$$[k] = \sqrt{(2/3)} * \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{2.2.2}$$

Similarly conversion for 3-ϕ instantaneous load currents,

$$\begin{bmatrix} i_o \\ i_\alpha \\ i_\beta \end{bmatrix} = [k] * \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \tag{2.2.3}$$

Where e_o,e_α and e_β are the equivalent instantaneous voltages in '0-α-β' co-ordinate system, and i_o, i_α and i_β are the equivalent instantaneous currents in '0-α-β' co-ordinate system. It is assumed that the source is balanced and hence the zero sequence voltage 'e_o' is equal to zero. Unless otherwise stated, the load is assumed to be balanced one and hence 'i_o' is equal to zero.

Representing the active and reactive powers in '0-α-β' co-ordinate system [1],

$$p_o = e_o * i_o. \tag{2.2.4}$$

$$p = e_\alpha * i_\alpha + e_\beta * i_\beta. \quad (2.2.5)$$

$$q = e_\alpha * i_\beta - e_\beta * i_\alpha. \quad (2.2.6)$$

where p_o, p and q represent the instantaneous zero sequence power, instantaneous active power, and instantaneous reactive power. Writing the above equation in matrix form,

$$\begin{bmatrix} p_o \\ p \\ q \end{bmatrix} = \begin{bmatrix} e_o & 0 & 0 \\ 0 & e_\alpha & e_\beta \\ 0 & -e_\beta & e_\alpha \end{bmatrix} * \begin{bmatrix} i_o \\ i_\alpha \\ i_\beta \end{bmatrix} \quad (2.2.7)$$

The instantaneous active power p, instantaneous reactive power q and the instantaneous zero-sequence power p_o are illustrated for a linear balanced load (CASE-I), nonlinear balanced load (CASE-II), and linear unbalanced load (CASE-III).

CASE - I :

Fig. 2.2. shows the variation of instantaneous active and reactive power under linear load consisting of R-L. The top figure shows the phase-a system voltage with a reduced scale of 1:20 ('ea/20') and the corresponding phase load current i_a. The middle figure shows the active power p where as the bottom figure shows the reactive power q of the load considered in this case. It is clear from this figure that p and q have only dc components and no alternating components are present.

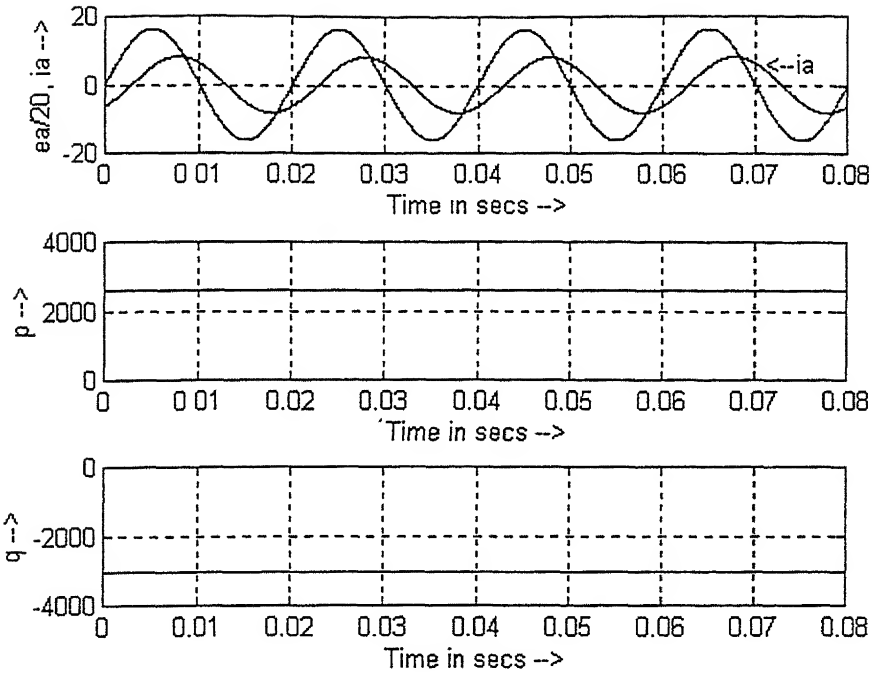

Fig. 2.2: p, q with linear & balanced load

CASE-II :

Fig. 2.3. shows the variation of p and q with non-linear load such as a controlled rectifier with zero delay angle. As in the previous case, the top part of the figure shows the load current i_a and '$e_a/20$', the middle one shows p and the bottom part shows q. It is evident from the figure that p and q each have both average and alternating components. Unlike in case-1, the alternating components are present though their mean value is zero.

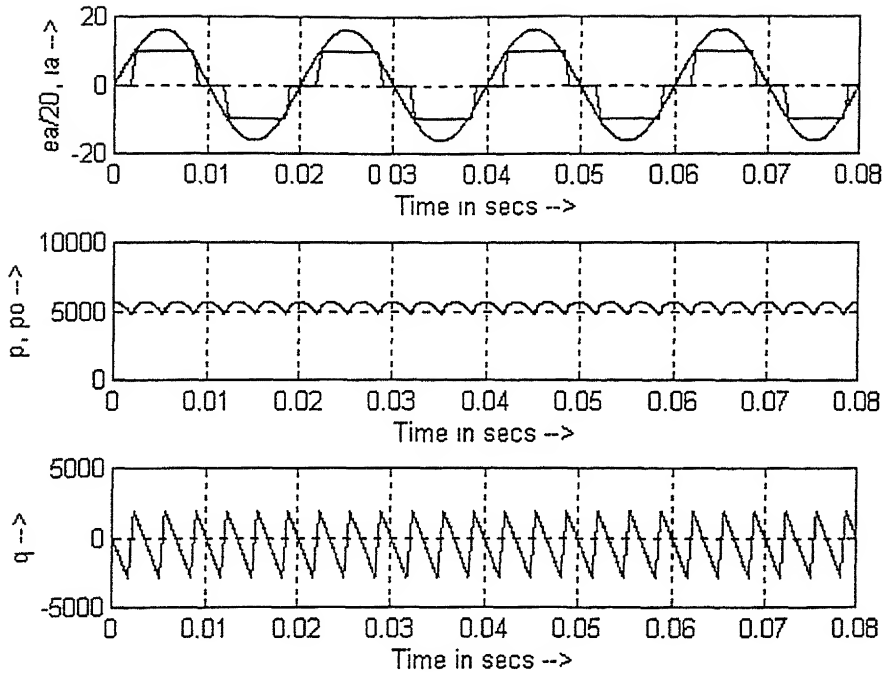

Fig. 2.3 : p, q with non-linear load

These alternating components are denoted as $\tilde{p}$ and $\tilde{q}$ for alternating active and reactive powers respectively, where as the average or dc components are denoted as $\bar{p}$ and $\bar{q}$ representing the average active and reactive powers respectively.

CASE-III :

Fig. 2.4 depicts the variation of p , q and p_o for linear unbalanced case of load. The top part shows that the 'phase-a' load current i_a is zero representing the unbalanced condition, the bottom part shows the instantaneous zero - sequence power p_o which is equal to zero .The middle two sub-figures show the instantaneous active and reactive powers p and q. Each of these powers have not only average but also alternating component. The frequency of these alternating components is not as high as that in CASE-II. But these alternating components have frequency even multiple of the fundamental frequency and thus symmetrical over the half cycle of the fundamental component.

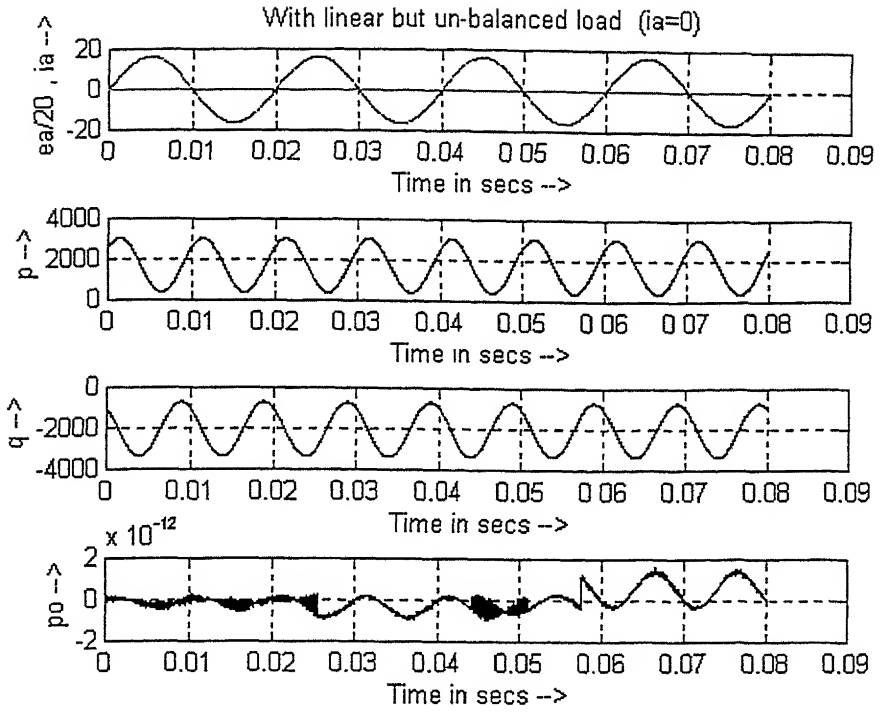

Fig. 2.4 : p, q , & p_o with linear but un-balanced load

Thus, from CASE-I, CASE-II and CASE-III it can be generalised that the instantaneous active power and instantaneous reactive power can be expressed as the sum of their instantaneous alternating components and instantaneous average components. In other words,

$$p = \tilde{p} + \bar{p}. \tag{2.2.8}$$

$$q = \tilde{q} + \bar{q}. \tag{2.2.9}$$

2.3 Moving Average Technique

The best way to determine the alternating components in p and q is to find out the average component in them and then subtract this from p and q [3]. Akagi used a butter-worth filter to find out the average component [3]. However this low-pass filter affects the compensation characteristics in transient states as the filter is having its own settling time.

The advancement in the area of processors has brought fast processors like DSP, which can be used to find out the average component. This is explained as follows.

Fig. 2.5 shows the block diagram of the moving average technique. The main purpose is to separate the two components in both p and q as explained earlier.

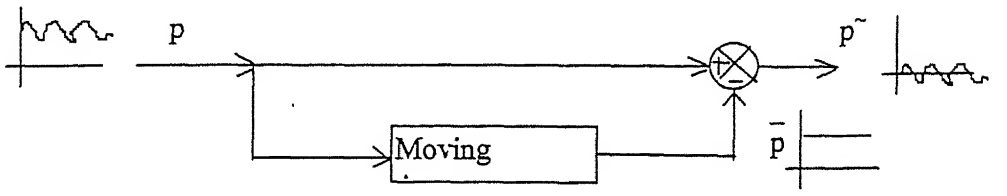

Fig. 2.5: Block diagram of the averaging circuit.

The averaging of p and q is performed over a period of half cycle of (0.01 s) of the system voltage as the wave forms of p and q repeat after every 0.01s both for linear unbalanced and nonlinear loads. A moving window is considered in which the latest sampled datas of p or q for the last 0.01s are added and the average is found out. After getting $\bar{p}$ and $\bar{q}$, these two quantities are subtracted from the values of p and q respectively thereby giving $p^{\sim}$ and $q^{\sim}$ instantaneously. To have better understanding of the moving averaging technique, it is further elaborated in the section that follows.

Let there be N number of sampling datas available in 0.01s, which of curse depends on the sampling frequency. Supposing that we are at the n_{th} sampling instant, then for n_{th} sampling instant,

$$\bar{p} = (1/N) * \sum_{i=(n-N+1)}^{i=n} (p_i). \qquad \text{when } n \geq N. \qquad (2.3.1)$$

and

$$\bar{p} = (1/n) * \sum_{i=1}^{i=n} (p_i). \qquad \text{when } n < N. \qquad (2.3.2)$$

However ,during the 1st half cycle time just after the load is applied or changed, the average found out is not the exact one, but it gives reasonable compensation during this 1st half cycle as shown in Section 2.4. Thus in the worst case an interval 0.01s is required to get the actual average from the instant the load changes. Henceforth, it is assumed that the load remains constant for at least an interval of 0.01s for meaningful compensation of reactive power.

Fig. 2.6 illustrates the effect of change of load on calculation of the average. In this figure there are three plots. The top one shows the phase-a load current i_a and the corresponding phase source voltage with reduced scale of 1:20. The middle figure shows the active power p denoted as P; the average active power $\bar{p}$ is denoted as Pdc: and the bottom figure shows the alternating active power $\tilde{p}$ which is denoted as Pac.

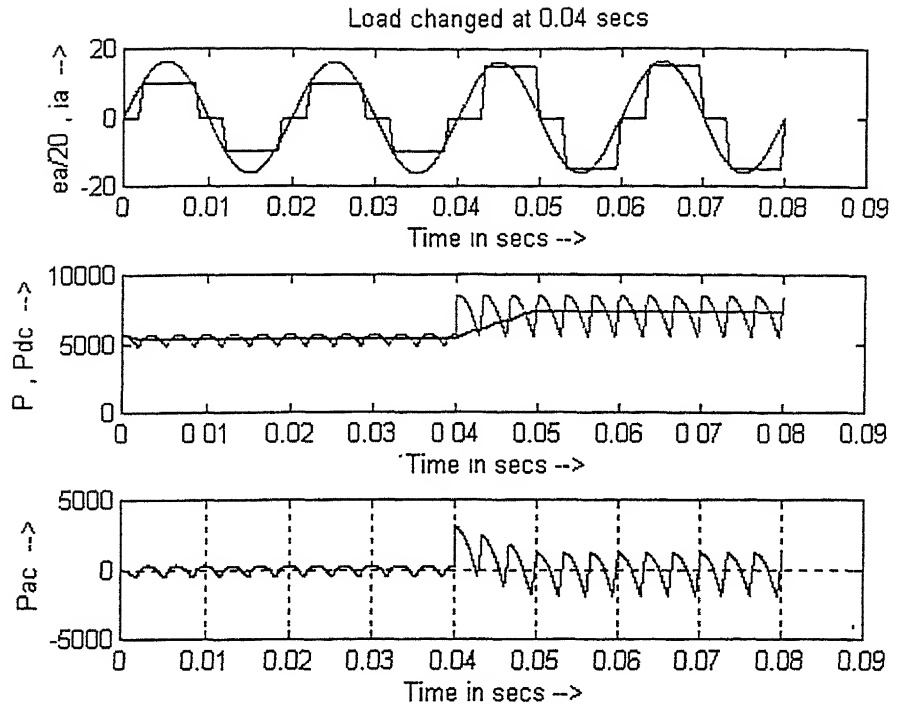

Fig. 2.6: Response of moving average technique.

Fig. 2.6 shows how instantaneous average value is derived from the instantaneous value of p .The rectifier load (delay angle = 0 degree) is applied at time t = 0, and is increased by 50 % with delay angle increased to 20^0 at time t = 0.04s. As clear from the above figure it takes 0.01s for the average quantity to settle down to new load conditions. During 0.04s to 0.05s also, the $\bar{p}$ is closer to the actual value which is occurring after 0.05s. In the next section , the effect of this moving averaging on the compensation characteristics is presented. It reveals the effectiveness of moving average technique to provide reasonable compensation during the transient period as well.

Once $\bar{p}$ and $\bar{q}$ are obtained , $\tilde{p}$ and $\tilde{q}$ for that instant are obtained according to the block diagram shown in Fig. 2.5. Therefore,

$$\tilde{p} = p - \bar{p}. \tag{2.3.3}$$

$$\tilde{q} = q - \bar{q}. \tag{2.3.4}$$

2.4 Reference Current Generator

For compensation of reactive power and current harmonics, it is required to supply the undesirable power components of the load from the compensator as shown in Fig. 2.1. These components would come from the source in the absence of compensation. The compensator in this case is connected in parallel with the system. Hence, the current at the point of common connection of the compensator takes care of the undesirable power components. The reference current generator generates the reference currents individually for taking care of individual power components shown in Fig. 2.1. The reference currents for each phase are generated as follows.

To compensate the power component $\tilde{p}$, the compensator reference currents in '0-α-β' co-ordinate system are

$$\begin{bmatrix} i_{c\alpha\tilde{p}}^{*} \\ i_{c\beta\tilde{p}}^{*} \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} * \begin{bmatrix} \tilde{p} \\ 0 \end{bmatrix} . \qquad (2.4.1)$$

Similarly to compensate the power component $\tilde{q}$ and $\bar{q}$, the compensator reference currents in '0-α-β' co-ordinate system are

$$\begin{bmatrix} i_{c\alpha\tilde{q}}^{*} \\ i_{c\beta\tilde{q}}^{*} \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} * \begin{bmatrix} 0 \\ \tilde{q} \end{bmatrix} . \qquad (2.4.2)$$

$$\begin{bmatrix} i_{c\alpha\bar{q}}^{*} \\ i_{c\beta\bar{q}}^{*} \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} * \begin{bmatrix} 0 \\ \bar{q} \end{bmatrix} . \qquad (2.4.3)$$

The compensator reference current due to the power component p_o , represented in '0-α-β' co-ordinate system is

$$i_{co}^{*} = i_o \,, \tag{2.4.4}$$

Where i_o is given by the equation 2.23 .

Thus the compensator reference currents from (2.4.1)-(2.4.4) are

$$\begin{bmatrix} i_{co}^{*} \\ i_{c\alpha}^{*} \\ i_{c\beta}^{*} \end{bmatrix} = \begin{bmatrix} i_o \\ i_{c\alpha p\sim}^{*} + i_{c\alpha q\sim}^{*} + i_{c\alpha \bar{q}}^{*} \\ i_{c\beta p\sim}^{*} + i_{c\beta q\sim}^{*} + i_{c\beta \bar{q}}^{*} \end{bmatrix} \tag{2.4.5}$$

The compensator reference currents due to all of the three power components (i.e. $p\tilde{}$, $q\tilde{}$, $\bar{q}$) , represented in 'a-b-c' co-ordinate system are

$$\begin{bmatrix} i_{ca}^{*} \\ i_{cb}^{*} \\ i_{cc}^{*} \end{bmatrix} = [k]' \begin{bmatrix} i_{co}^{*} \\ i_{c\alpha}^{*} \\ i_{c\beta}^{*} \end{bmatrix} \tag{2.4.6}$$

Equation (2.4.6) gives the value of instantaneous compensator reference currents which should be supplied by the compensator so as to compensate the reactive power caused by the fundamental and /or the harmonic currents depending upon the applications. Under perfect compensation, the compensator is assumed to supply the reference currents given by (2.4.6). The source currents will then be given by

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} i_{ca}^{*} \\ i_{cb}^{*} \\ i_{cc}^{*} \end{bmatrix}. \tag{2.4.7}$$

Equation (2.4.7) is obtained as per the convention shown in Fig. 2.1 . The source currents under ideal compensation are obtained by taking a controlled rectifier load with a delay angle of 20 degrees into consideration. The effect of individual power

components on the source currents is studied. Each case is illustrated with a figure which contains three sub-figures showing i_a, i_{ca}^*, i_{sa}^*. Also, the phase-a source voltage with a reduced scale of 1:20 is shown as 'ea/20' in all these cases.

Fig. 2.7 shows the effect of compensating $\bar{q}$ only on the source current. It is quite evident from the sub-figure c that the source current i_{sa}^* has its fundamental component in phase with the source voltage, but it contains harmonics. Thus, it is clear that compensating $\bar{q}$ only makes the displacement factor unity. The current harmonics are still present in the source current. Fig. 2.8 shows the effect of compensating $\tilde{q}$ only on the source current for the same load. It is revealed that $\tilde{q}$ is responsible for contaminating the source current with harmonics , as the compensation of only this component filters the harmonics considerably from the source current. This is clear from the sub-figure c of Fig. 2.8, i_{sa}^* has improved considerably from the presence of harmonics.

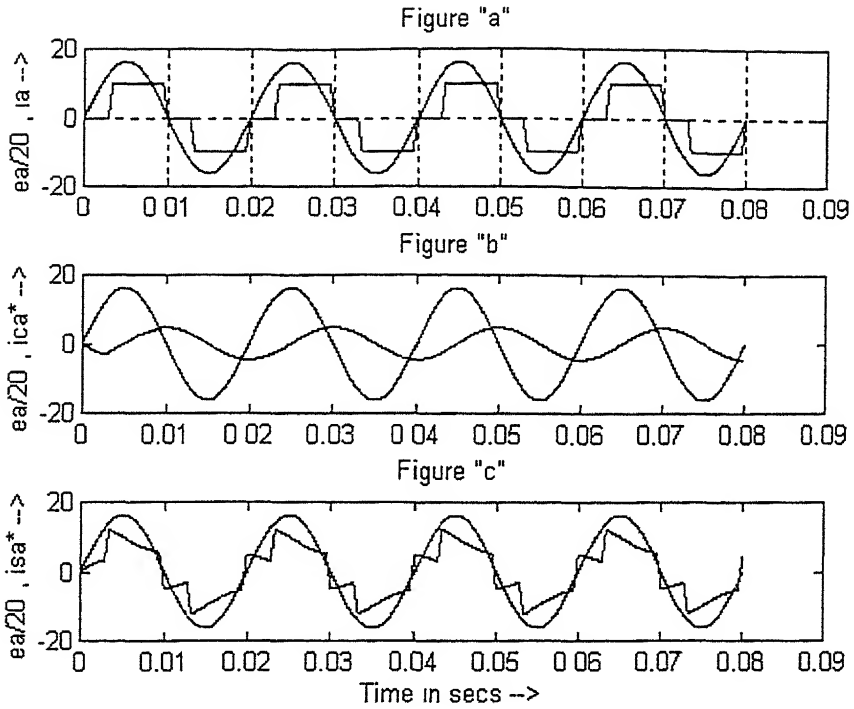

Fig. 2.7: i_{ca}^* and i_{sa}^* when only $\bar{q}$ is compensated.

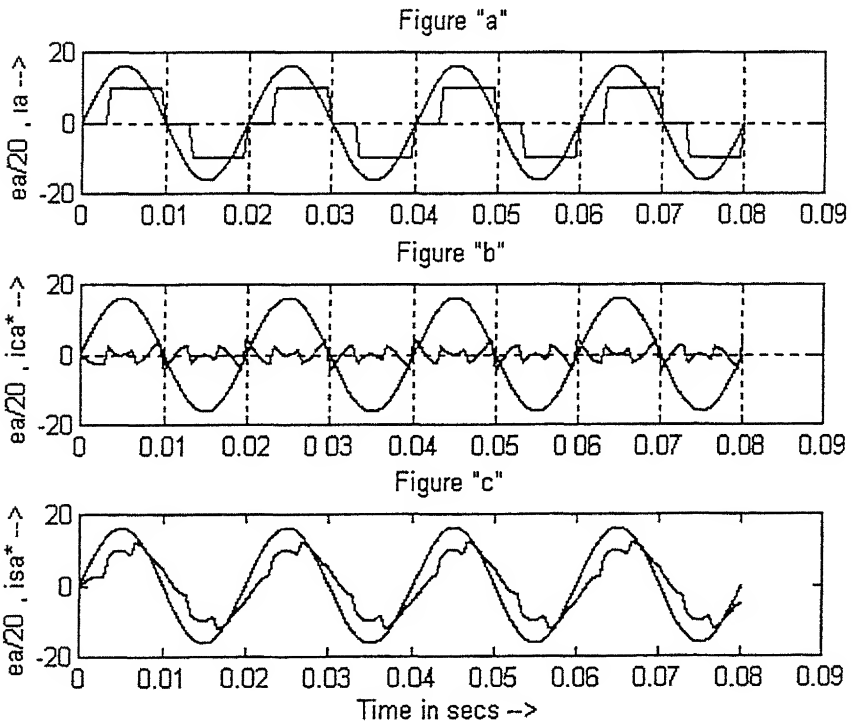

Fig. 2.8: i_{ca}^* and i_{sa}^* when only $\tilde{q}$ is compensated.

Fig. 2.9 reveals that compensation of $p^{\sim}$ alone leads to compensation of current harmonics partly from the source. Further it does not improve the displacement fator similar to compensation of $q^{\sim}$. In this case the source current i_{sa}^{*} almost resembles the load current. But it eliminates the current harmonics though in a small amount. Figure 2.10 shows the effect of compensating both $p^{\sim}$ and $q^{\sim}$. This results in complete elimination of current harmonics from the source current . The source current i_{sa}^{*} in sub-figure c of Fig. 2.10 is perfectly sinusoidal but it lags behind the supply voltage e_a with the same angle as the fundamental component of the load current. Therefore, the power '$p^{\sim} + q^{\sim}$' is regarded as Harmonic Power, the compensation of which eliminates all the harmonics from the source current.

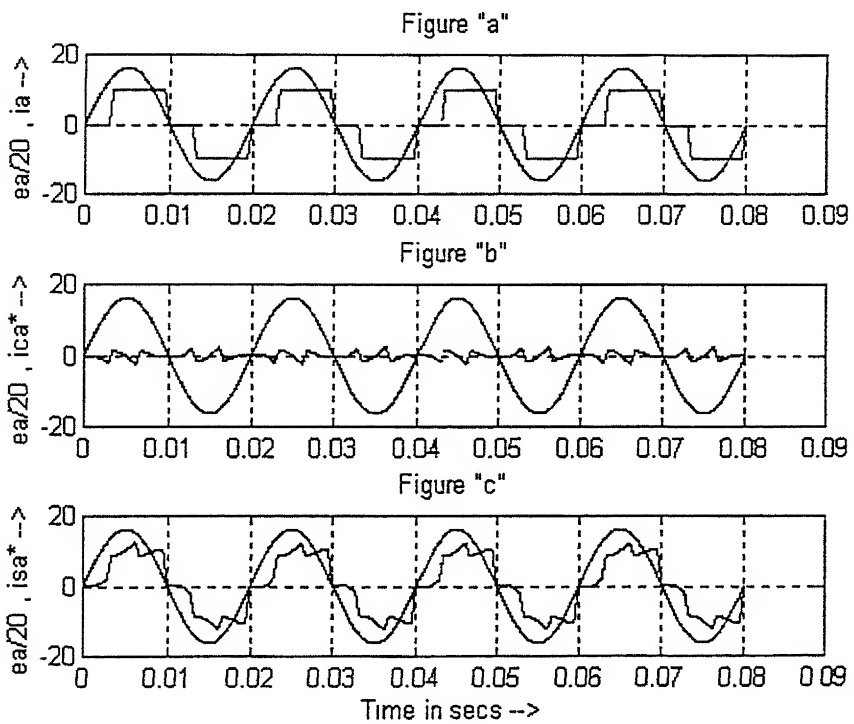

Fig. 2.9: i_{ca}^{*} and i_{sa}^{*} when only $p^{\sim}$ is compensated.

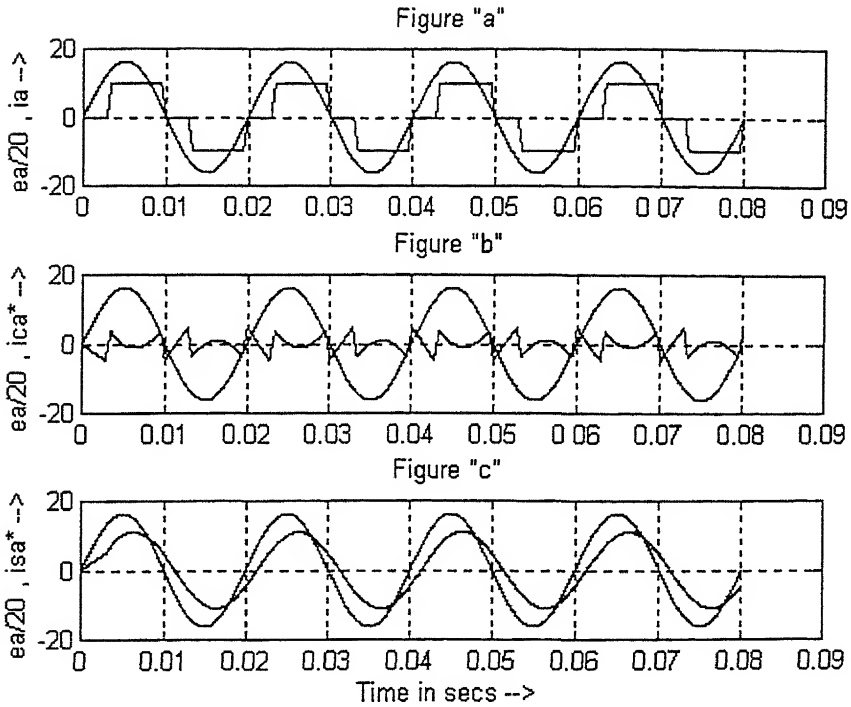

Fig. 2.10: i_{ca}^* and i_{sa}^* when harmonic power $(\tilde{p} + \tilde{q})$ is compensated.

Where as in Fig. 2.11 the source current is perfectly sinusoidal and in phase with the source voltage resulting complete elimination of harmonics and unity displacement factor. However the source current is not perfectly sinusoidal during the 1st half cycle because the moving average output is not exactly equal to the actual average during this 0.01 s.

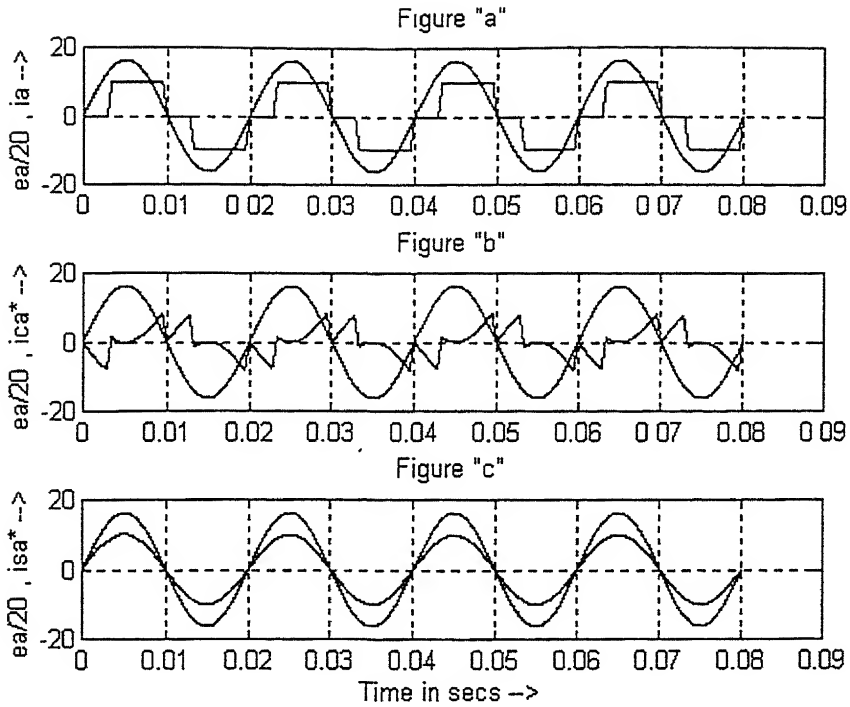

Fig. 2.11: i_{ca}^* and i_{sa}^* when $(\bar{q} + \tilde{p} + \tilde{q})$ is compensated.

The effectiveness of the moving average technique is studied under transient condition of load change. This is illustrated in Fig. 2.12. The load is taken to be the same as in Fig. 2.32 in which only average and alternating powers 'Pdc' and 'Pac' are depicted with the load increased by 50% at 0.04s.The transient response and the effectiveness of moving average technique could be seen from the wave form of i_{sa}^* of Fig. 2.12. During the transient periods when the load is applied initially (i.e. 0.0 to 0.01s) and also when the load is changed subsequently (0.04 to 0.05s) the source current is not perfectly sinusoidal until the transient period is over. However the current is almost sinusoidal during the transient period also.

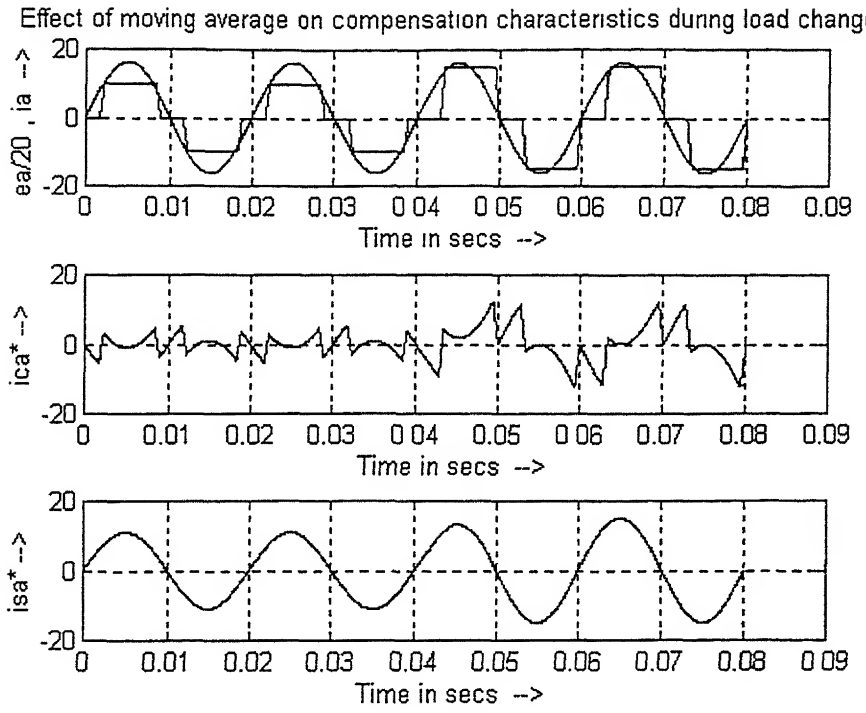

Fig. 2.12: i_{ca}^* and i_{sa}^* during load transient (load increased by 50% at 0.04 secs).

2.5 Conclusion

Thus it can be concluded that $\tilde{p}$ and $\tilde{q}$ contribute to the current harmonics present in the source current, and hence together called as Harmonic Power. Contribution of $\tilde{q}$ towards harmonics is much greater than that of $\tilde{p}$. In case the application requires complete elimination of current harmonics from the supply system, $\tilde{p}$ and $\tilde{q}$ have necessarily to be compensated. The reference currents are then determined considering $\tilde{p}$ and $\tilde{q}$ only and setting $\bar{q}$ to zero. However, the compensation of $\tilde{q}$ only results partly elimination of current harmonics. The compensation of $\bar{q}$ only makes the displacement factor unity. The importance of the terms $\tilde{p}$, $\tilde{q}$, $\bar{q}$ for achieving instantaneous reactive and harmonic power compensation has been explained in this chapter.

The source current i_{sa}^* throughout this chapter is found out by assuming that the compensator supplies its reference current i_{ca}^* . Theoretically It is possible to make the source current of desired shape by appropriately choosing the compensator current i_{ca}^* .Therefore, the effectiveness of "instantaneous reactive and harmonic power compensation" depends on how well the compensator follows its reference currents. This aspect of making the compensator to follow its reference currents using current controllers is discussed in Chapter 3 that follows.

Chapter 3

CURRENT CONTROLLERS

3.1 Introduction

The instantaneous reactive power compensation and current harmonics elimination involves the instantaneous injection of particular current to the system. As shown in the previous chapter the reference currents contain harmonics. Thus the compensator generates harmonic currents of desired shape and feeds it to the system to nullify the effect of reactive power demanded by the load.

It is easier to control the current with Voltage Source Inverter (VSI) than with a Current Source Inverter(CSI). Single-phase and three-phase bridge type voltage source inverters operated by either dc source or capacitors are used as compensators. The topologies of inverters used also includes multi-level inverters specially for high power applications with improved wave forms. The details of multilevel inverters are presented in Chapter 4.

Waveshaping the desired current with these topologies of VSIs requires a current controller, which derives the switching signals for the inverter. Figure 3.1 shows the block diagram of a typical compensator which performs reactive power compensation and harmonic current minimisation or elimination. This is achieved by current control technique. The desired reference currents are set for the compensator and the object is to see that the compensator provides these currents. This is achieved through current controllers. Ultimately, it is the current controller block which makes it possible to closely follow the

reference currents. This is in fact is the subject of this Chapter. Bang-Bang hysteresis current control with variable switching frequency and current control with constant switching frequency are presented in this Chapter.

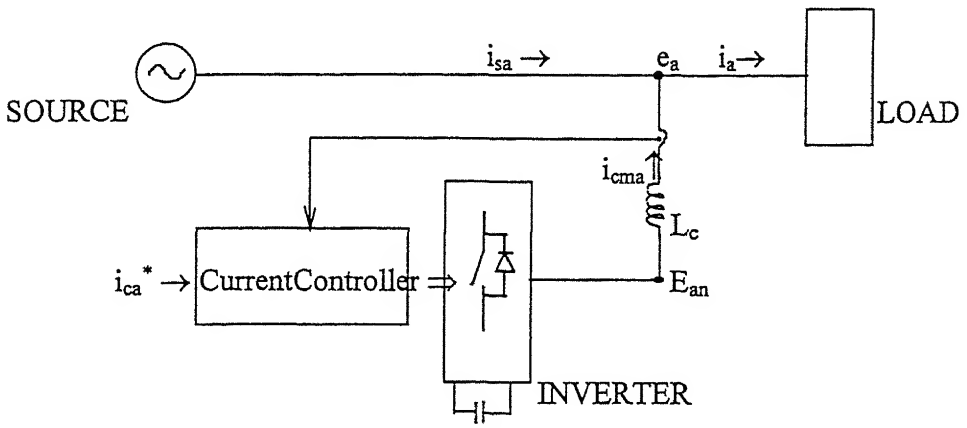

Fig. 3.1: Block diagram of the Compensator showing Current controller.

The block diagram in Fig. 3.1 shows single line diagram representing only phase-a quantities. L_c is the interfacing inductance between the inverter and the supply system. It is to be kept small for fast response of the compensator. E_{an} is the inverter output voltage of phase-a. i_{ca}^* is the phase-a compensator reference current derived as in Chapter 3. i_{cma} is the phase-a current injected to the system from the compensator. The current controller requires instantaneous value of the reference current and the actual phase a current. Two such current controllers for the other two phases are required for deriving the switching signals for a three-phase inverter. The inverter will then be switched to provide the necessary output voltages there by making the actual currents follow the reference currents.

The most common and effective among the current control techniques is the Bang-Bang Hysteresis technique. It is the simplest technique with excellent current tracking capability. But the serious drawback with this is that the switching frequency varies within a wide range over each half cycle of the input system voltage. Lower is the band better is the

current tracking but higher becomes the switching frequency. This becomes a problem in high power level where maximum number of switchings over a period is to be limited. Going for a small value of interfacing inductance to have faster response and smaller size of inductor results in further increase of switching frequency. Since the switching frequency is not constant, it results in non-uniform heat loss thereby increasing the stresses on devices and heat-sink as well. Then the device and heat sink should be designed for the maximum switching frequency which occurs only for small intervals during each half cycle of input system voltage. This results in under utilisation of switching devices and heat sinks.

To overcome these disadvantages of the bang-bang hysteresis technique, current control is obtained with the inverter operating at constant switching frequency. In this constant switching frequency current control, the inverter is forced to operate at a predetermined frequency and the current is allowed to vary within an imaginary band by choosing proper value of inductance. Even with a low value of inductance, the switching frequency can be held at the predetermined value.

A detailed comparison of results with these two current control techniques is presented in this chapter. A three level 3-ϕ inverter is used to inject currents that follow the reference currents. The working of this three level inverter is presented in Chapter-4.

3.2 Constant Switching Frequency Technique

Constant switching frequency is accomplished by generating a triangular wave of frequency equal to the desired switching frequency as applied to buck-boost converter for current waveshaping [4]. The reference currents as found out in Chapter 2 are then added to this triangular wave, thus creating new reference currents for the inverter given by

$$i_{car} = i_{ca}^{*} + i_{trg} . \quad (3.2.1)$$

$$i_{cbr} = i_{cb}^{*} + i_{trg} . \quad (3.2.2)$$

$$i_{cbr} = i_{cb}^{*} + i_{trg} . \quad (3.2.3)$$

where i_{trg} is the triangular wave of desired switching frequency . The magnitude of this triangular wave forms an imaginary band similar to the hysteresis band in case of bang-bang current control. This is illustrated in Fig. 3.2. The triangular wave (i_{trg}) is generated at 10khz frequency as shown in Fig. 3.2(a). This i_{trg} is then added to the reference current i_{ca}^* to get the new reference current i_{car} which is shown in sub-figure b. This i_{car} creates an imaginary band equal to twice the magnitude of the triangular wave as clear from the sub-figure b.

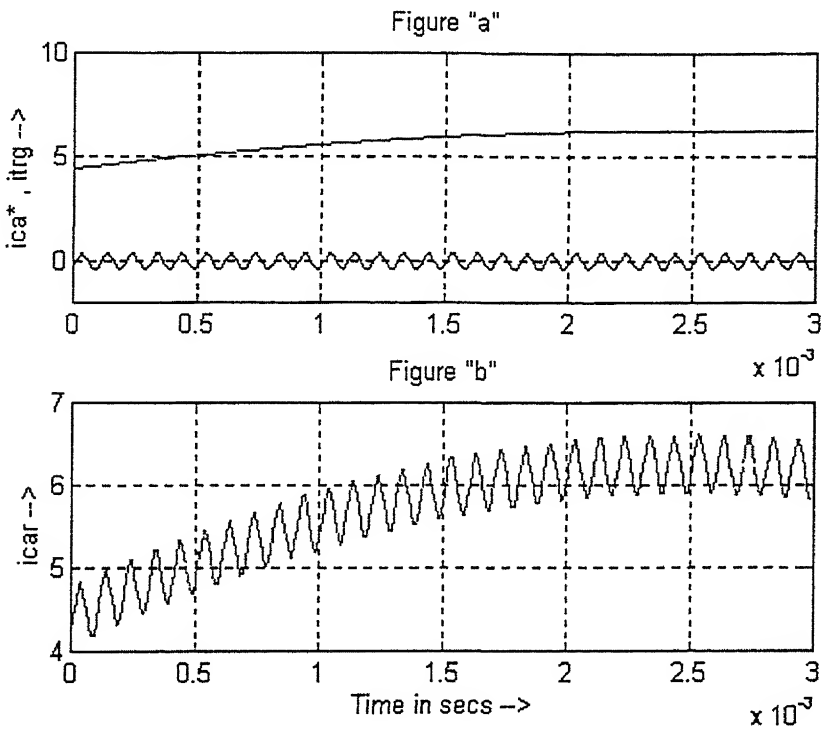

Fig. 3.2: Deriving the new reference current.

Fig. 3.3 shows the action of the current controller to obtain constant switching frequency. This figure reveals that the current controller derives the ON signal (A=1) when the actual current i_{cma} meets the positive slope of the reference current i_{car} indicating that the current i_{cma} needs to be increased. Here, A=1 indicates that the inverter

should be switched in such a way as to increase i_{cma} . Similarly when i_{cma} meets the negative slope of i_{car} , OFF signal (A=0) is derived by the controller indicating that i_{cma} needs to be decreased. Thus the driving signals are derived once during each slope making the switching frequency constant throughout the operation of the inverter. Also, the current error is confined to be inside the imaginary band created by the triangular wave as illustrated in Fig. 3.3.

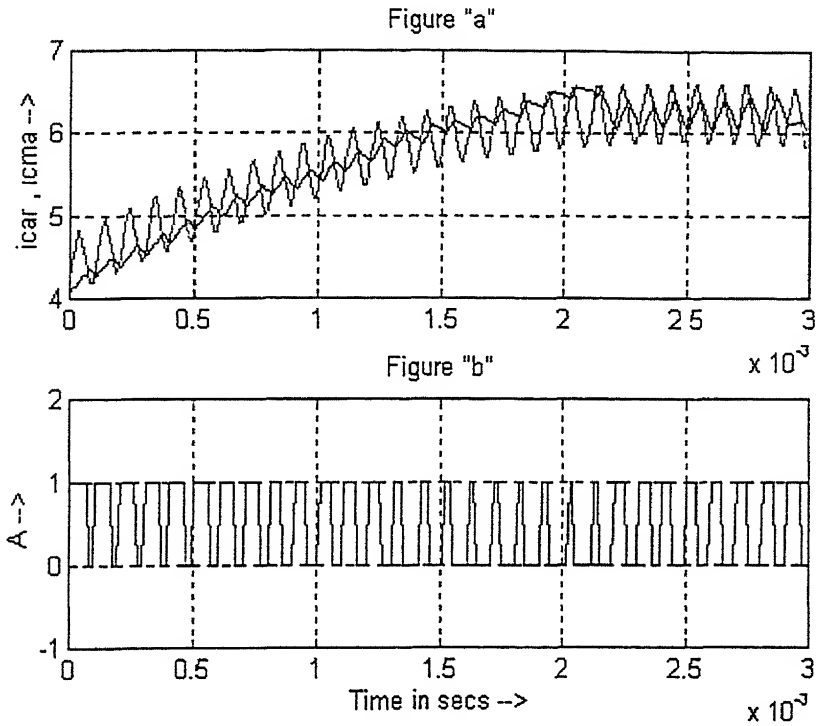

Fig. 3.3: Showing the current controller action.

For proper operation of this current controller, the inductance L_c should be such that the maximum slope of the current i_{cma} should be less than the slope of the triangular wave. This ensures that the current error is always within the imaginary band. Taking this aspect in view the value of the inductance is calculated as follows.

$$(\Delta i_{cma} / \Delta t)_{max} = 4 * f_c * \delta. \qquad (3.2.4)$$

where δ is the magnitude of the triangular wave and f_c is the frequency of the triangular wave equal to the desired switching frequency f_{sw}.

$$L_c * (\Delta i_{cma} / \Delta t) = (E_{an} - e_a). \quad (3.2.5)$$

Thus from (3.2.5)

$$(\Delta i_{cma} / \Delta t)_{max} = (E_{an} - e_a)_{max} / (L_c)_{min} \quad (3.2.6)$$

From (3.2.4) and (3.2.6) the minimum value of inductance is

$$L_c = |(E_{an} - e_a)|_{max} / (4 * f_c * \delta). \quad (3.2.7)$$

(3.2.7) is also valid for bang-bang hysteresis control with δ equal to upper or lower band and f_c equals to the desired maximum switching frequency. The value of inductance found in (3.2.7) is large enough for most of the intervals during each half cycle of the input system voltage. This is so as $|(E_{an} - e_a)|_{max}$ occurs only for small intervals during each half cycle of e_a. Thus this value of inductance makes response slower and unsuitable for fast changing slopes of load currents like rectifier load.

This is illustrated in Fig. 3.4, which is obtained by using a three level inverter operating at 10 kHz. δ is taken to be 8% of the maximum load current. Thus L_c is taken to be 15 mH satisfying (3.2.7). Controlled rectifier load with 20^0 delay angle is considered here. Fig.3.4 shows that the inductance is high enough for some regions resulting in discrepancies between i_{car} and i_{cma}.

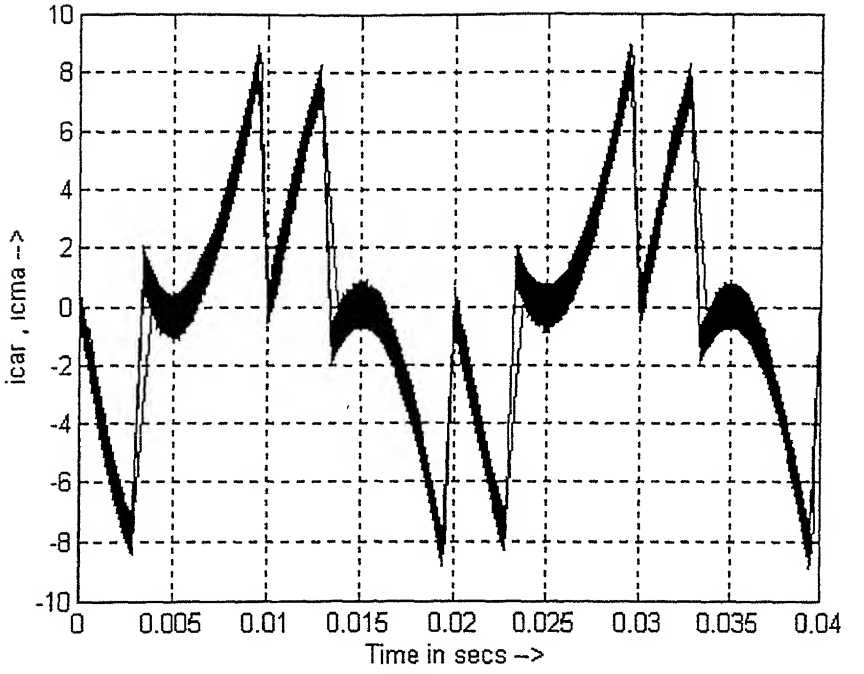

Fig. 3.4: Showing the effect of L_c on i_{cma}.

The effect of this mismatch is reflected in the source current i_{sa} which increases by around 40% of the maximum load current during that region as illustrated in Fig. 3.5. The situation will be worst in case of three level if it is required to apply positive E_{an} when e_a is at its negative peak for the purpose of increasing the current or to apply negative E_{an} when e_a is at its positive peak in order to decrease the current.

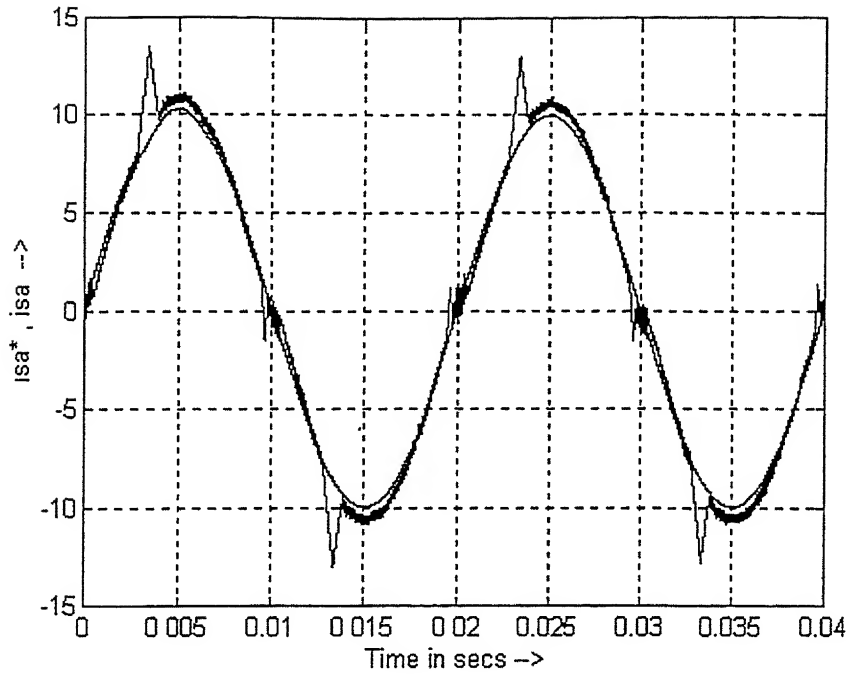

Fig. 3.5: Showing the effect of L_c on i_{sa}.

Thus it is better to go for an inductance lower than that found by (3.2.7) letting the current error cross the imaginary band in some regions. This makes the response faster and reduces the size of the inductor as well. But due to this lower value of inductance the current i_{cma} may not meet the next slope of i_{car} in some intervals because of the reason that the slope associated with i_{cma} at those intervals is more than that of i_{car}. To take care of this situation additional features are added for the current controller to derive the switching signals.

- No change in the driving signal (A) takes place only when 'sl'>0 and $\Delta i_c >$ 0' or

'sl < 0 and $\Delta i_c < 0$'.

- For all other cases , A = 1 when sl > 0 and A = 0 when sl < 0.

Where sl = slope of the triangular wave, $\Delta i_c = i_{cma} - i_{car}$ and A is the driving signal from the current controller. The driving signal could be derived by using the logic gates as shown in Fig. 3.6 where x and y represent the binary form of sl and Δi_c respectively.

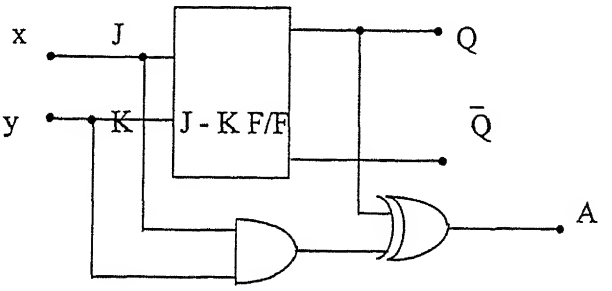

Fig. 3.6 : Deriving the driving signal 'A' using logic gates.

The current controller with this added features is now capable of providing constant switching frequency even with a value of L_c lower than that found in (3.2.7). It has been shown latter in this chapter that the results are better than that in Figs. 3.4 and 3.5 with L_c equal to 8 mH with other parameters remaining the same.

3.3 Comparison of Bang-Bang and Constant Switching Frequency Techniques

Comparison of results among the two types of current control techniques is performed for a controlled rectifier load with 20^0 of delay angle. The switchings that take place over a half cycle is shown in both the cases. The desired switching frequency is taken to be 10 kHz for this rectifier load.

The constant switching frequency technique described already allows to go for a inductance L_c lower than that in (3.2.7). It is found that with δ equals to 8% of the maximum load current and f_c equals to 10 kHz, the constant switching frequency technique provides reasonable compensation even with L_c as low as 8 mH. This is illustrated in Fig. 3.7. The sub-figure "c" in this figure shows the switching signal A corresponding to phase -

a. The other sub-figures are self explanatory. The sub-figure shows that the response is faster as i_{cma} matches with i_{car} at almost every part of the half cycle of e_a. It is evident that i_{cma} is crossing the imaginary band during some regions.

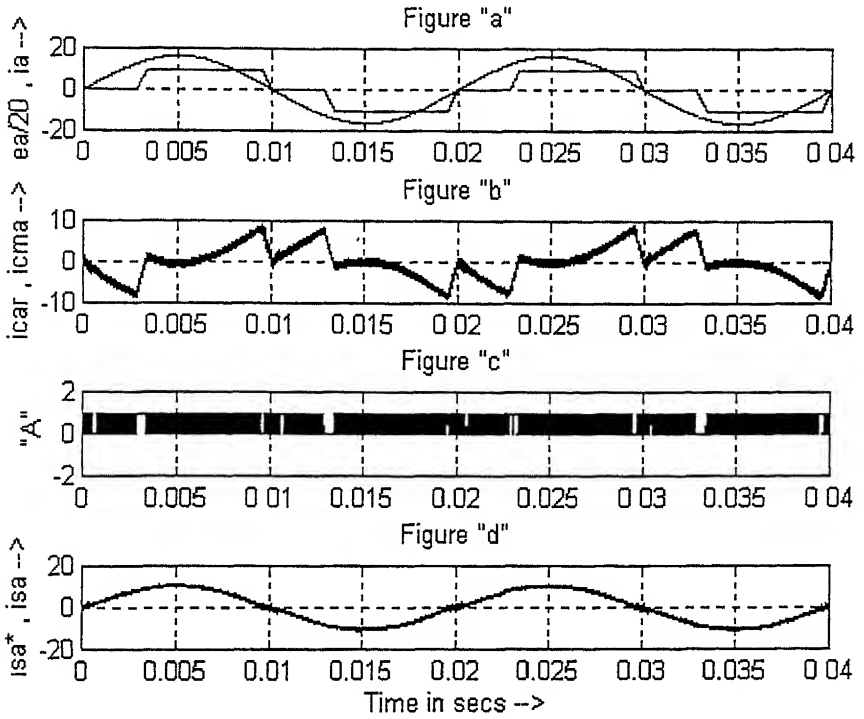

Fig. 3.7 : Response of Constant Switching Frequency Technique.

With the same parameters the results are obtained with bang-bang current control and illustrated in Fig.3.8. This figure could be compared with Fig. 3.7. No doubt the source current has a better shape and confined within the band in Fig. 3.8. But looking to the sub-figure "c" , it is clear that the switching frequency varies over a wide range. Some regions are densed while the other regions are not so indicating that the device is under utilised.

Later in this section, the details of the switching pattern and the tracking of the current of both of these techniques are analysed over a half cycle.

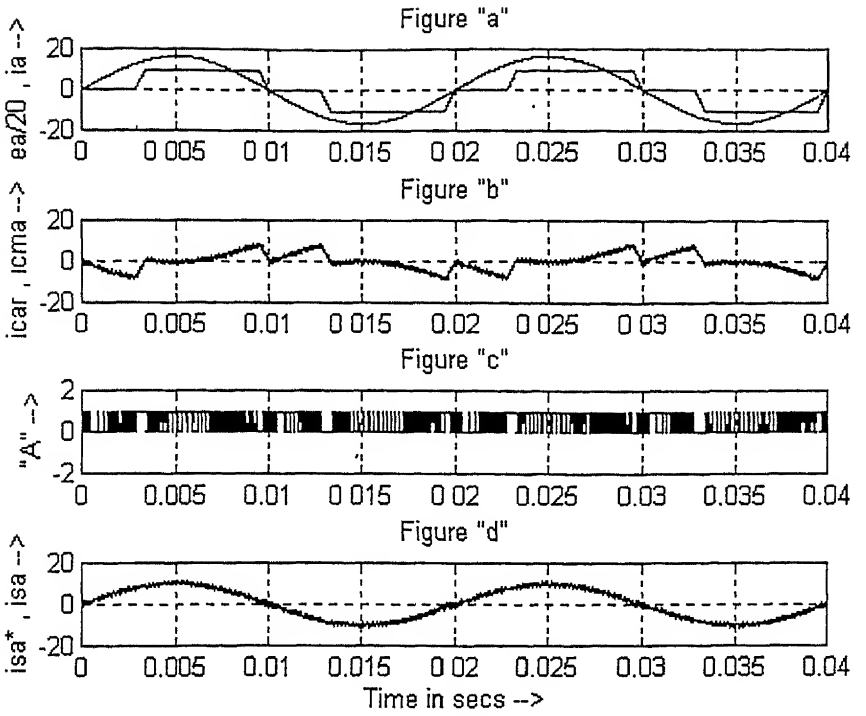

Fig. 3.8 : Response of bang-bang hysteresis technique.

Figs.3.9 and 3.10 shows the response of bang-bang and constant switching frequency technique respectively over a quarter cycle (0.02s to 0.025s). This clearly shows how switching signal A is derived in both techniques.

Fig. 3.9 (a) shows that going for a low value of inductance makes the response faster. Fig. 3.9 (b) reveals that the rate at which switchings take place is not uniform even during a quarter cycle. It is maximum near 0.02s and less in other regions. The rate at which the switchings take place throughout the cycle is presented later in this chapter.

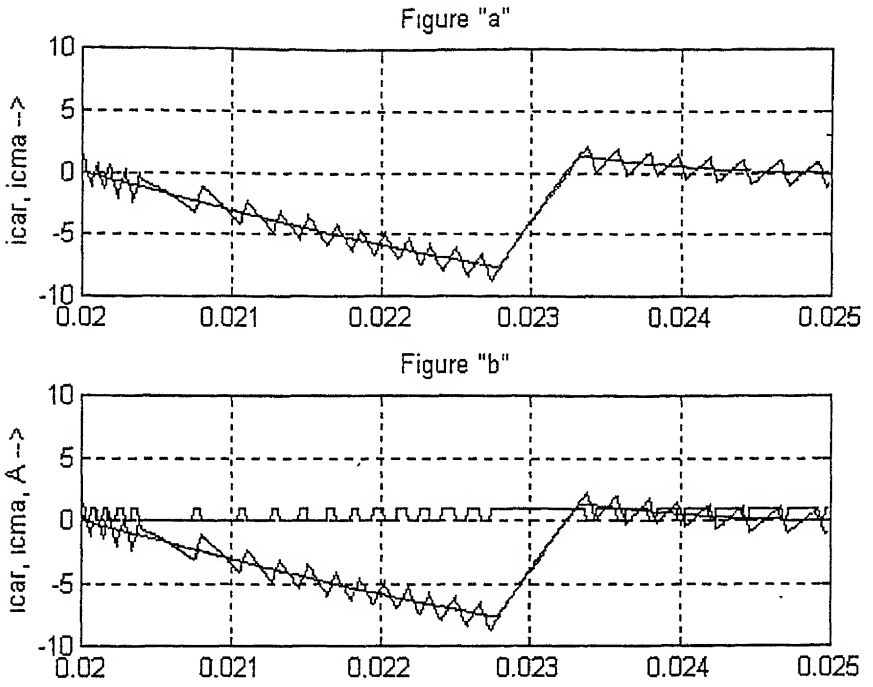

Fig. 3.9 : Response of bang-bang hysteresis technique.

In Fig. 3.10 with constant switching frequency, the switchings are almost uniform and equals to f_c except during the intervals when there is fast changes in i_{car}. From Fig. 3.10 (b) it is clear that the added logic to the control technique works successfully. In some regions (near 0.02s) the current crosses the imaginary band while switching frequency still remains the same, thus allowing the use of a lower value of inductance. It is clear that in most of the regions the current i_{cma} remains within the imaginary band.

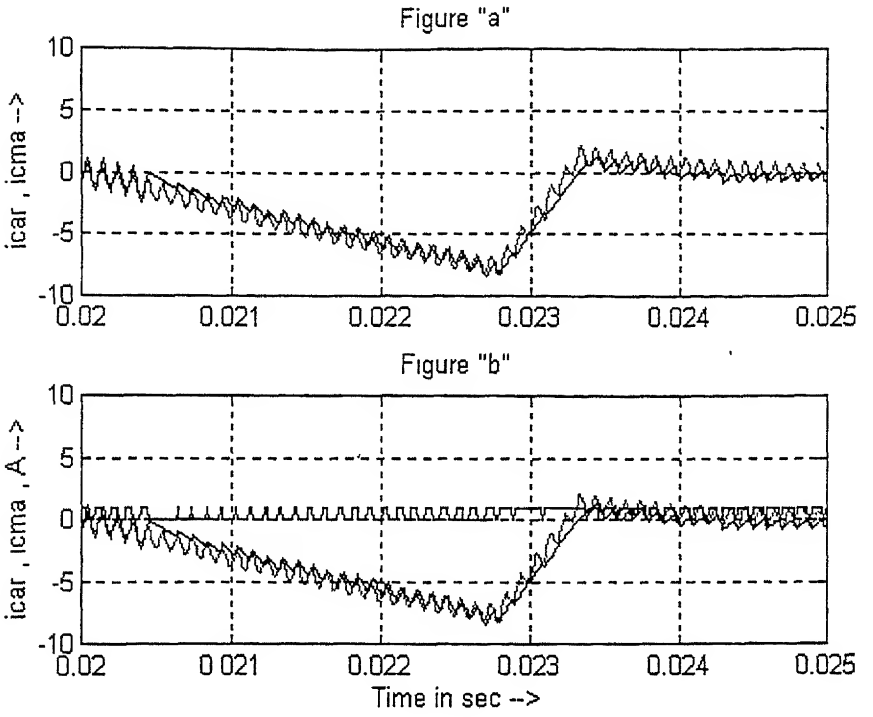

Fig. 3.10 : Driving Signal (A) with Constant Switching Frequency Technique.

Fig. 3.11 and Fig. 3.12 shows the responses of bang-bang and constant switching frequency techniques respectively for the next quarter cycle (0.025s to 0.03s).

Fig. 3.11 again reveals that the switchings take place at a higher rate only in small regions near 0.03s and it varies over a wide range even in this quarter cycle. The tracking of reference current is not proper when sharp change of i_{car} takes place during 0.029s to 0.03s.

The results are better in case of constant switching frequency during this quarter cycle as shown in Fig. 3.12. The current i_{cma} is always within the imaginary band except for a short period near 0.03s.

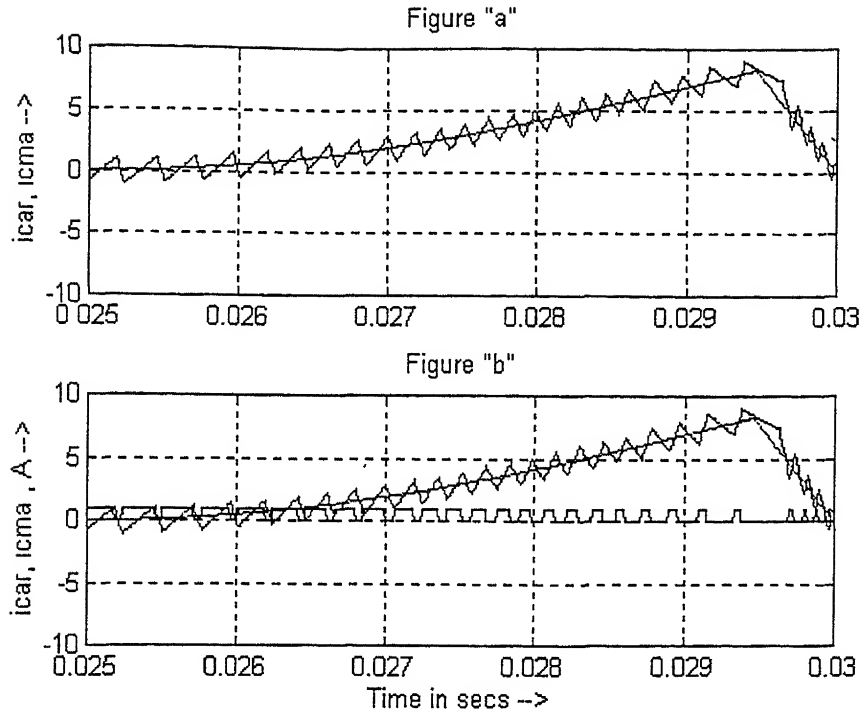

Fig. 3.11 : Driving Signal (A) with Bang-Bang Hysteresis Technique.

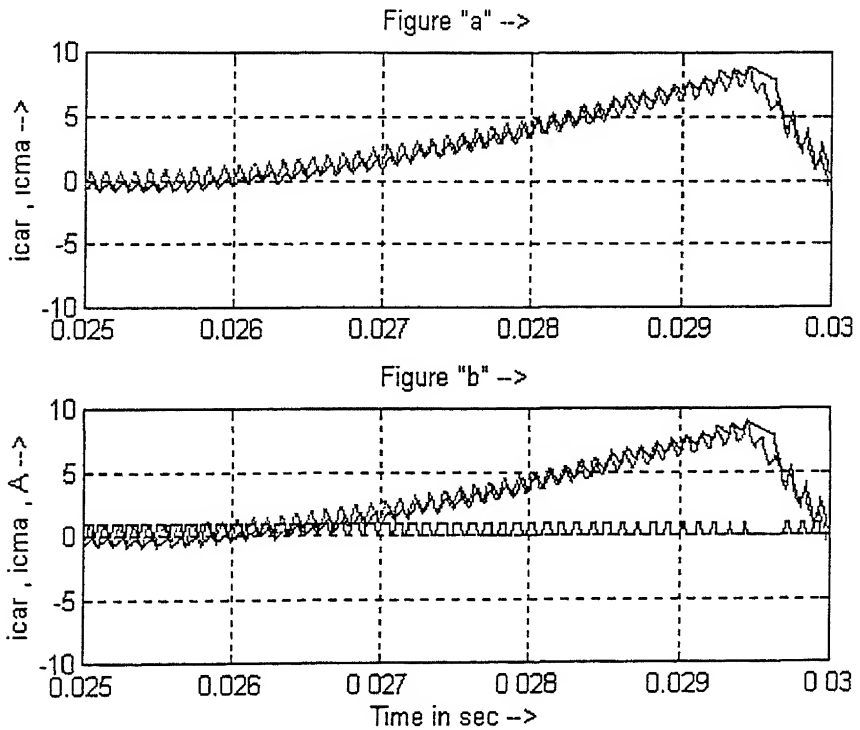

Fig. 3.12 : Driving Signal (A) with Constant Switching Frequency Technique.

Thus it is clear from the above comparison the switching frequency varies over a wide range during each half cycle of e_a and the current i_{cma} always remains within the specified band in case of bang-bang hysteresis current control technique. In the technique employing imaginary band, the switching frequency is almost constant in each half cycle of e_a. However, the current i_{cma} crosses the imaginary band for some short intervals only. This crossing of the band occurs due to selection of a lower inductance for making the response faster. The rate at which the switchings are taking place using bang-bang technique is found out from (3.2.7) and shown in Fig. 3.13 consisting of three sub-figures. The inverter output voltage E_{an} is shown in the middle figure and the rate of switchings 'f_{sw}' is shown in the bottom figure. It is clear from this figure that by choosing a lower value of inductance to make the response faster, the maximum switching frequency goes as high as 15 kHz whereas it is 10 kHz in constant switching frequency case.

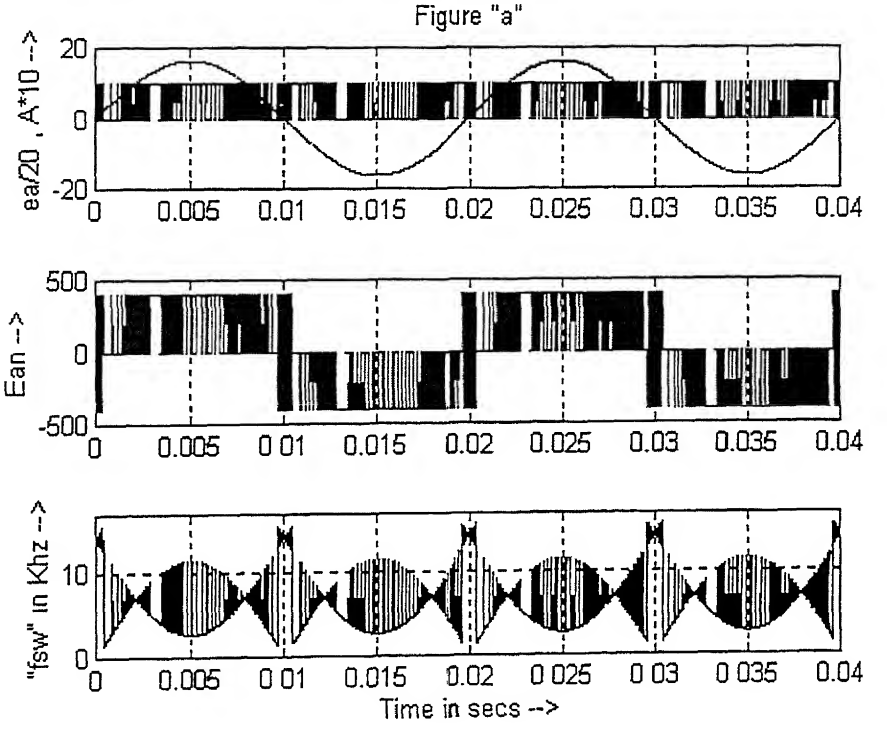

Fig. 3.13 : Variation of switching frequency f_{sw} in case of bang-bang technique.

Now there are two ways of making the maximum switching frequency to come down to 10 kHz. One way is to increase the band and the other one is to choose a higher value of inductance keeping other parameters constant. The effect of these two aspects are presented as follows.

To limit the maximum switching frequency to 10 kHz, δ alone is increased to 12% of the maximum load current. The results are then shown as in Figs. 3.14 and 3.15. It is clear from these figures that the maximum switching frequency is occurring over a small interval in each half cycle while the frequency is much lower than 10 kHz over rest of the intervals in each half cycle. It will result in under utilisation of a device. Moreover, the fluctuation of current is increased to 12%.

This will deteriorate the source current besides increasing the current ratings of devices.

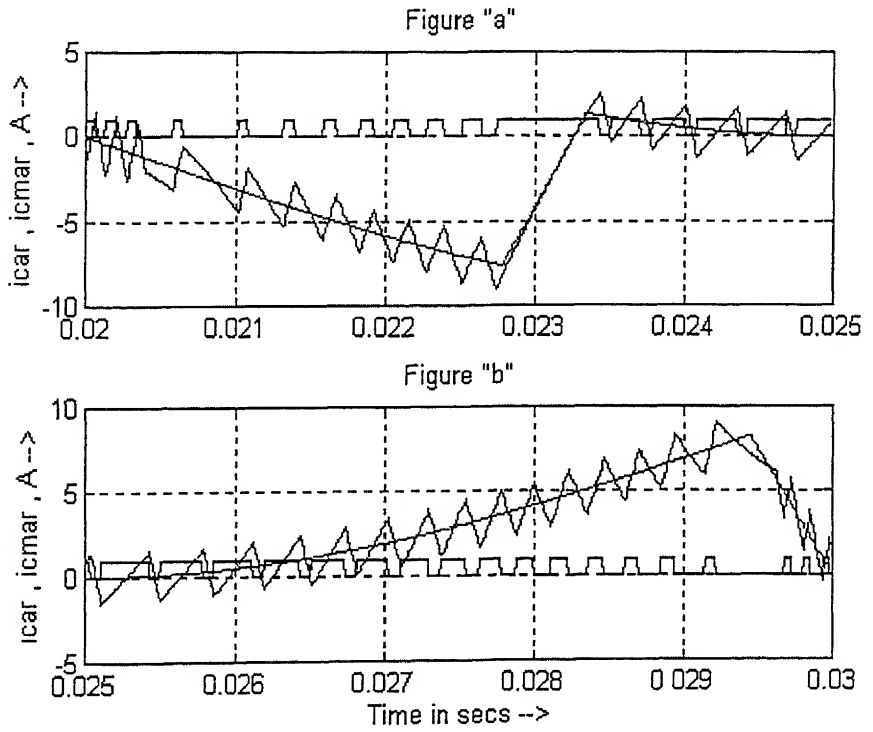

Fig. 3.14 : Response of bang-bang technique with increase of δ.

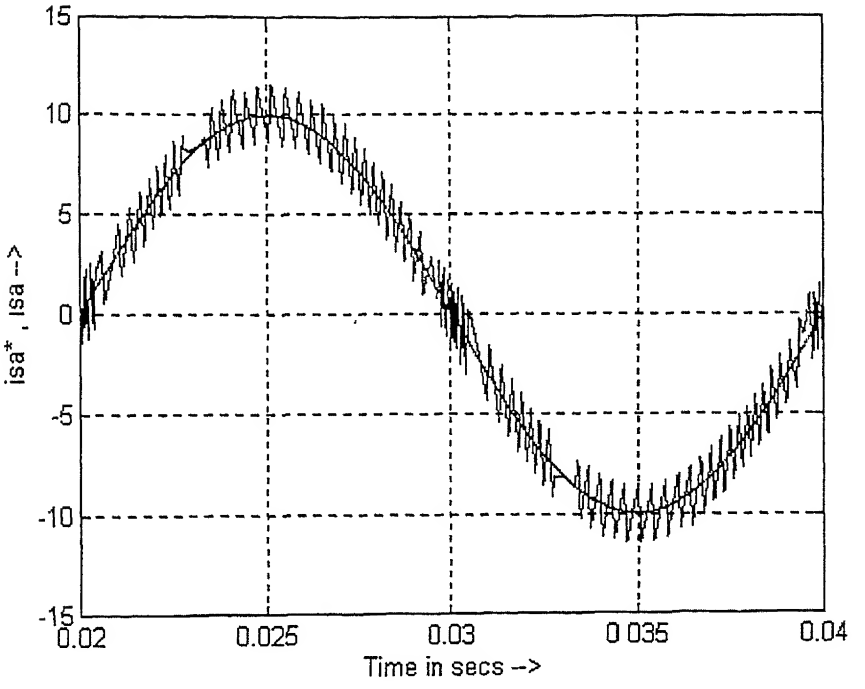

Fig. 3.15 : Source Current when δ increased to 12% of maximum load current.

Similarly to limit the switching frequency to 10kHz with a δ of 8%, the value of inductance is found to be 12 mH. Results are obtained with this value of inductance and shown in Figs.3.16 and 3.17. It is clear from these figures that the response becomes slower because of higher value of inductance than used in the constant frequency case.

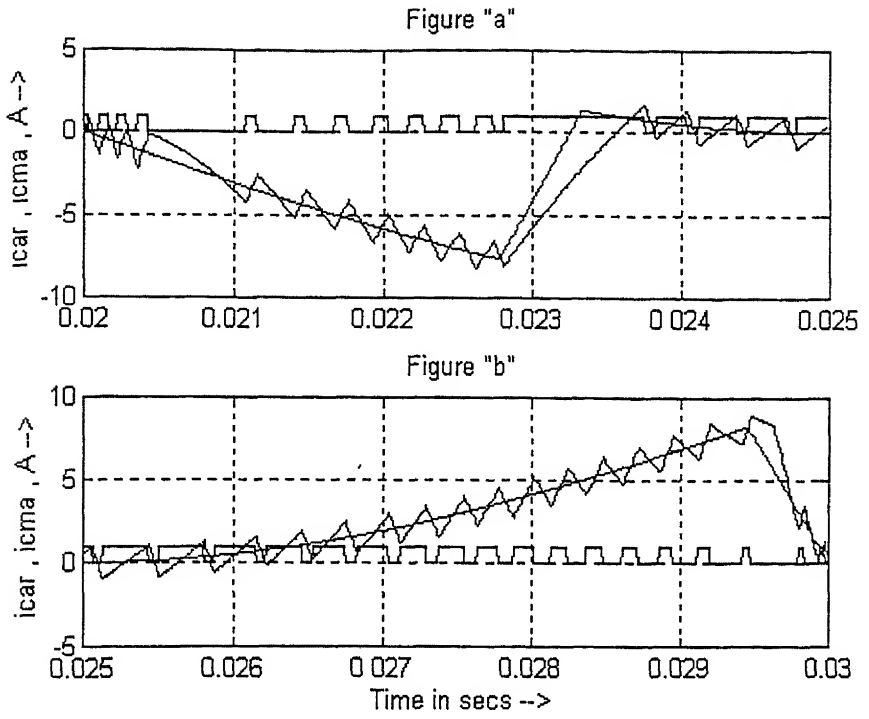

Fig. 3.16 : Response of bang-bang technique when inductance increased to 12 mH.

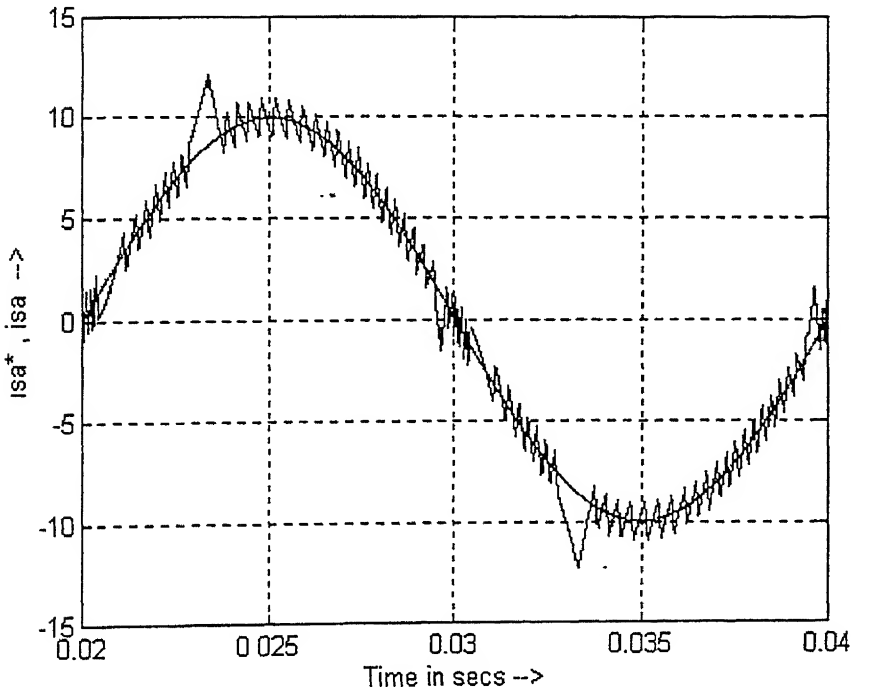

Fig. 3.17 : Source Current with inductance increased to 12 mH.

It has been shown that any attempt to limit the maximum switching frequency with bang-bang hesteresis technique creates problems of either increasing the current fluctuation or making the response slower. However with constant switching frequency for the same load current, and the same imaginary band it is possible to use a lower value of inductance.

The source current is shown in Fig. 3.18 with a δ of 8% of the maximum load current, f_c of 10 kHz and inductance of 8 mH. The source current is the same as shown previously in Fig. 3.7 (d), but shown for one cycle only for the sake of clarity.

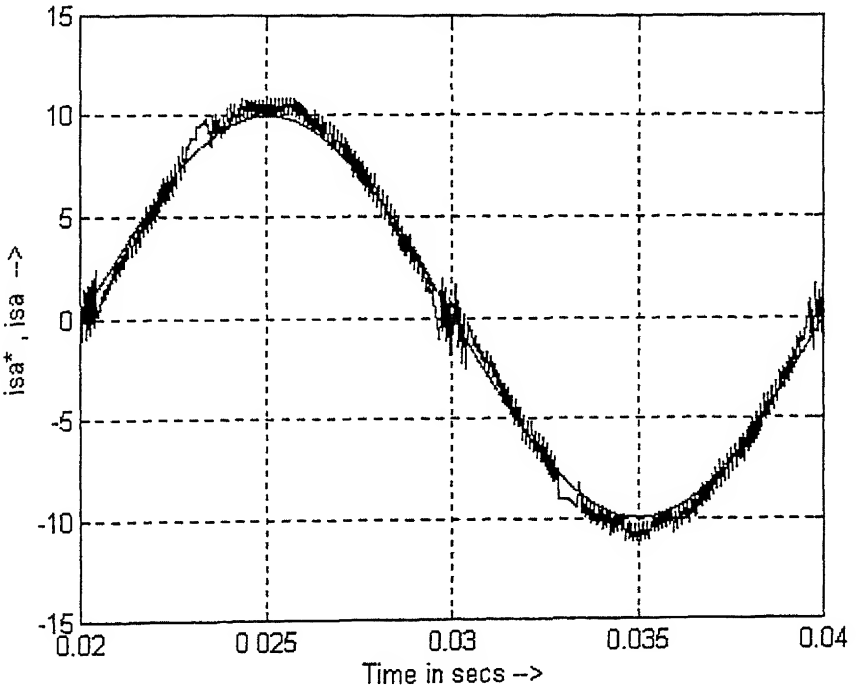

Fig. 3.18 : Source Current with Constant Switching Frequency Technique.

Though the source current in this case is not as good as that in bang-bang but it is quite reasonable from compensation point of view. To justify this point, the frequency spectrum of Fig. 3.18 for the compensated source current with constant switching frequency

technique is shown in Fig. 3.19. This reveals that from compensation point of view also, this constant frequency switching technique provides good results.

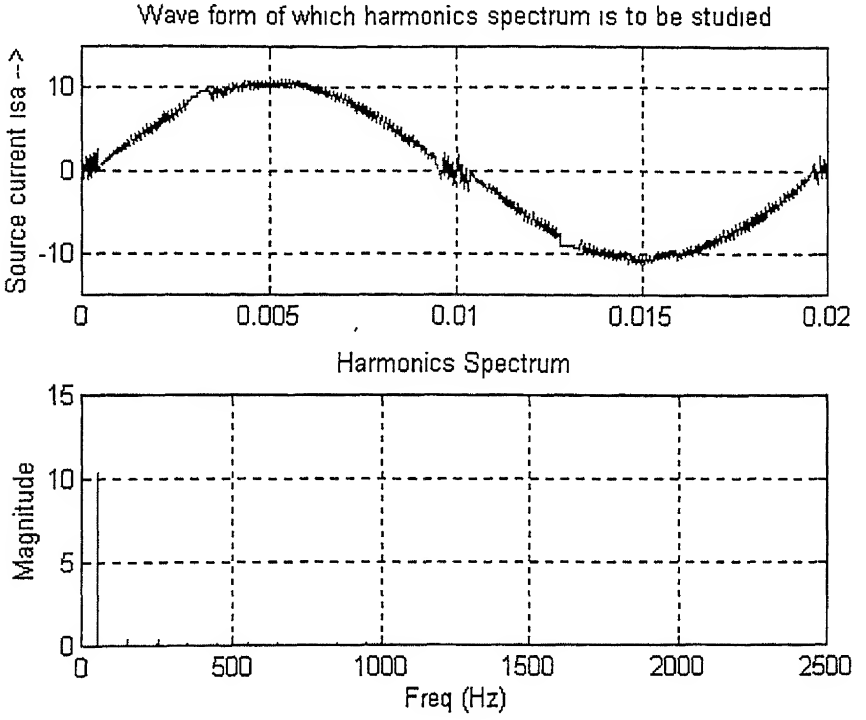

Fig. 3.19 : Harmonic Spectrum of Source Current i_{sa} with Constant Switching Frequency Technique.

3.4 Conclusion

From the studies presented in this Chapter, the constant switching frequency current control technique provides better features in terms of uniform switching losses for the devices, lower inductance, smaller compensator for a given rating, faster response etc. As the source current has a high frequency component of a particular frequency, the design of a filter becomes easier. This is, however, not the case with bang-bang hysteresis technique as the source current in this case contains components of different high frequency components. It has been shown that with the two current signals and some logic gates, the compensator can be designed to operate at constant frequency with lower inductance than in the case of Bang-Bang hysterisis control under similar operating conditions.

This Constant Switching Frequency Technique is used for the instantaneous reactive power compensation. The reactive and harmonic power compensation is obtained with different types of inverters such as single-phase inverters and two-level as well as multilevel three-phase inverters. All the topologies of inverters employ constant switching frequency current control technique. The topologies of three-phase inverters and their effectiveness to compensate reactive and harmonic power is presented in the next Chapter.

Chapter 4

COMPENSATION WITH THREE - PHASE INVERTERS

4.1 Introduction

The most common among the three phase inverters, used for reactive power compensation, is the three phase two level bridge type inverter. Coupling transformers are invariably used with this inverter for high power applications to mitigate power handling capabilities of the power semiconductor devices. Furthermore, the high power operation in such compensation schemes require parallel connection of the voltage source inverters [3]. Such configurations increase the cost and complexity of power circuits. Multi-level inverters have been used to meet the high power level [6] - [8] operating at high voltage supply without a coupling transformer. In this chapter, instantaneous reactive power compensation and harmonic power elimination is obtained with three phase multi-level (2, 3 and 5). The inverters are operated at constant switching frequency. The compensated source currents, switching signals for each phase, total harmonic distortion and capacitor voltage variations are presented for two-level, three-level and five-level inverters. Both balanced and unbalanced loads are considered.

4.2 Compensation with Two-level Inverter

Figure 4.1 shows the three phase inverter comprising of six switching devices and a capacitor in the dc side. The six switches namely k_{a1}, k_{a2}, k_{b1}, k_{b2}, k_{c1}, k_{c2} make the inverter operate as a three phase inverter. The capacitor is initially charged to a suitable voltage V_{c1}. E_{an}, E_{bn} and E_{cn} are the inverter output phase voltages. Each of these three phases can attain either + V_{c1} or - V_{c1} depending upon whether a switch in the top group (k_{a1}, k_{b1}, k_{c1}) or bottom group (k_{a2}, k_{b2}, k_{c2}) turns on. The inverter thus operates at two levels. There are two modes of operation of the inverter for each phase. Phase-a operation is described here which is applicable to other two phases also.

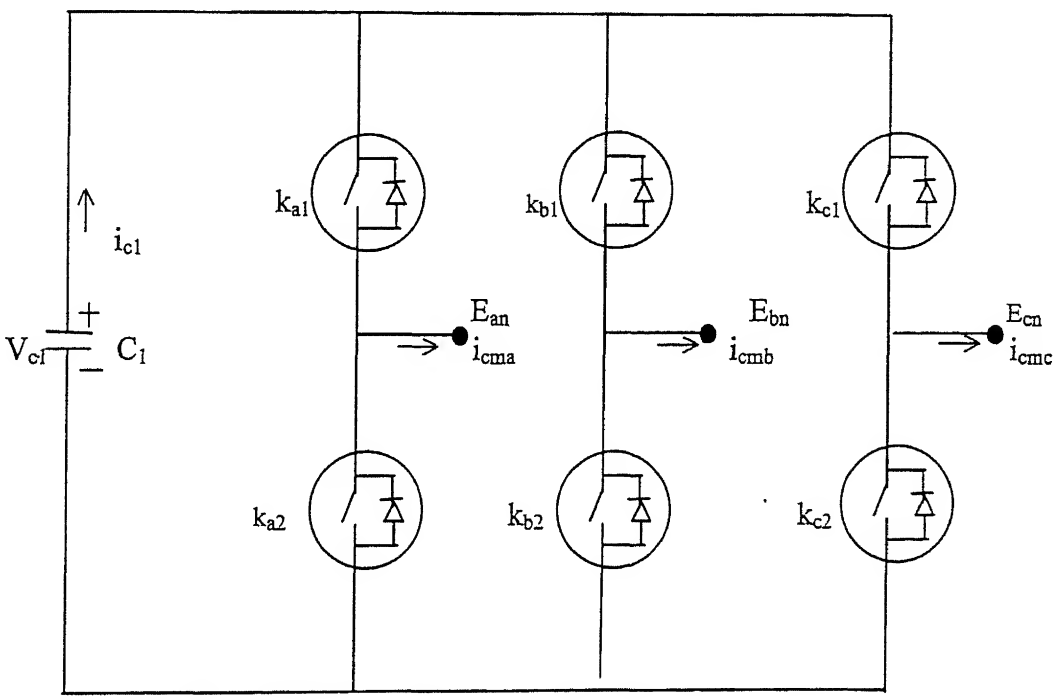

Fig. 4.1 : Configuration of two level inverter used.

Mode 1 :

When k_{a1} is 'on' and k_{a2} is 'off' indicating the necessity of applying positive voltage to phase-a at the inverter output. This situation arrives when the phase-a driving signal from the controller becomes high (A = 1), indicating that the phase-a current i_{cma} needs to be increased. In this mode of operation the top switch k_{a1} being ON takes care of both positive and negative phase-a currents. Positive i_{cma} flows through the device whereas negative i_{cma} flows through the diode connected across the switch k_{a1}.

Mode 2 :

The bottom switch k_{a2} is ON and the top switch k_{a1} is OFF when the current controller derives the phase-a signal as zero (A = 0) implying that the i_{cma} is to be decreased. In this mode also both positive and negative currents are taken care of by the diode and the device respectively

Similarly for other two phases, the top switches (k_{b1} and k_{c1}) of the phases are ON when the corresponding phase driving signals(B and C) becomes one. Like phase-a driving signal A, phase-b and phase-c driving signals are denoted as B and C. These signals are derived by the current controller that has already been described in the last chapter. From the instantaneous sensed values of load currents and system voltages, instantaneous reference currents for each phase are found out as explained in Chapter 2. These instantaneous reference currents are then compared with the sensed instantaneous output currents from the inverters by the current controller employing constant switching frequency technique as explained in Chapter 3. The controller derives the signals A, B and C and then each phase of the inverter is switched to either operate in Mode 1 or Mode 2 depending on the conditions described in both modes of operation. This in fact changes the inverter output voltages E_{an}, E_{bn} and E_{cn} such that the currents i_{cma}, i_{cmb} and i_{cmc} follow their respective phase reference currents thus satisfying the requirement of compensation.

The following equations govern the instantaneous operation of the inverter. The phase output voltages of the inverter are

$$E_{an} = (V_{c1} / 3) * (2 * A - B - C). \quad (4.2.1)$$

$$E_{bn} = (V_{c1} / 3) * (2*B - C - A). \quad (4.2.2)$$

$$E_{cn} = (V_{c1} / 3) * (2 * C - A - B). \quad (4.2.3)$$

The instantaneous phase currents from the inverters are then obtained from the following three equations.

$$L_c * (di_{cma} / dt) = E_{an} - e_a. \quad (4.2.4)$$

$$L_c * (di_{cmb} / dt) = E_{bn} - e_b. \quad (4.2.5)$$

$$L_c * (di_{cmc} / dt) = E_{cn} - e_c. \quad (4.2.6)$$

The instantaneous capacitor current i_{c1} and voltage V_{c1}, which are then calculated as in (4.2.7) and (4.2.8).

$$i_{c1} = (A * i_{cma} + B * i_{cmb} + C * i_{cmc}). \quad (4.2.7)$$

$$V_{c1} = - (1 / C_1) * \int i_{c1} * dt. \quad (4.2.8)$$

Assuming that the inverter operates in 180^0 mode of operation, V_{c1} always appears between the lines. Hence it is required that V_{c1} should be more than the maximum line to line system voltage. As the rms value of the system voltage is taken to be 400 volts, V_{c1} is initially charged to 700 V before the inverter is operated. L_c is 8 mH and δ is 8% of the maximum load current. Results of compensation with this inverter are obtained by considering both balanced and unbalanced cases. This is explained in two cases as follows.

CASE 1 :

A balanced controlled rectifier load with a delay angle of 20^0 is considered. Results obtained in this case are illustrated in Fig. 4.2. It is clear from sub-figures b that the inverter current i_{cma} follows its reference i_{car}. Since both these currents coincide in the figure. they are not seen separately. The source current as represented by the sub-figure c is almost free from harmonics. It is also seen to be in phase with the source voltage for the phase-a of subfigure a. Since the load is balanced, similar results are obtained for other two phases.

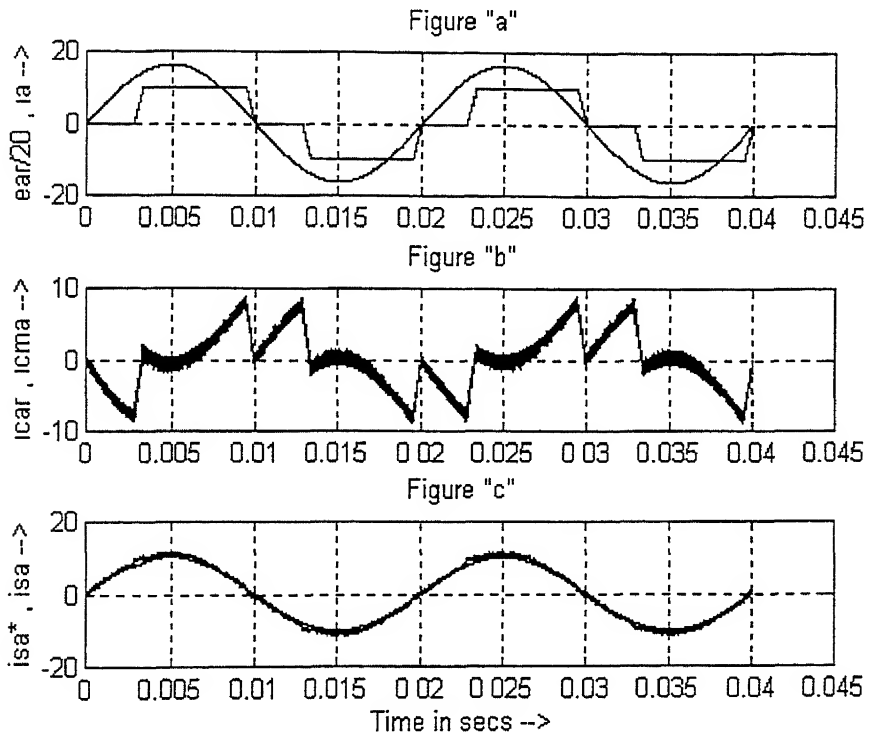

Fig. 4.2 : Results with balanced load.

CASE 2 :

The load is made unbalanced by making the phase-a load current i_a equal to zero. The other two phase load currents remain the same. The wave forms for this condition are illustrated in Fig. 4.3.

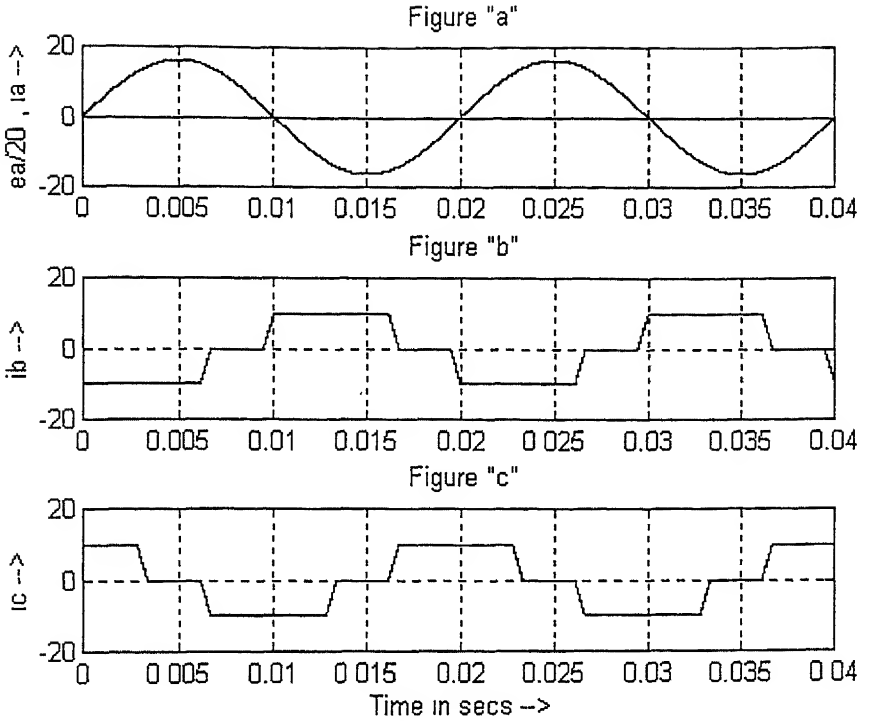

Fig. 4.3 : Load currents causing an unbalanced situation.

The results of compensation are obtained in case of this unbalanced load conditions and shown in Fig. 4.4. The three phase source currents i_{sa}, i_{sb} and i_{sc}, as seen from the figure do not depict balanced conditions. Though it is able to shape the phase-a current, it fails to shape the currents for the other two phases. This is the inherent drawback of this configuration of the two-level inverter. The reason for this could be explained by analysing the expressions for inverter output voltages given in (4.2.1) - (4.2.3). It is clear from these equations that each of the phase output voltages depend on the switching conditions of the other two phases also. For example, if A is equal to 1 indicating that the current is to be increased, the output voltage E_{an} is still dependent on B and C , which may result in making E_{an} zero if each of both B and C becomes 1. Thus, this makes the inverter fail to operate. Therefore this configuration of two level inverter is not suitable for the purpose of compensation, particularly for unbalanced loads.

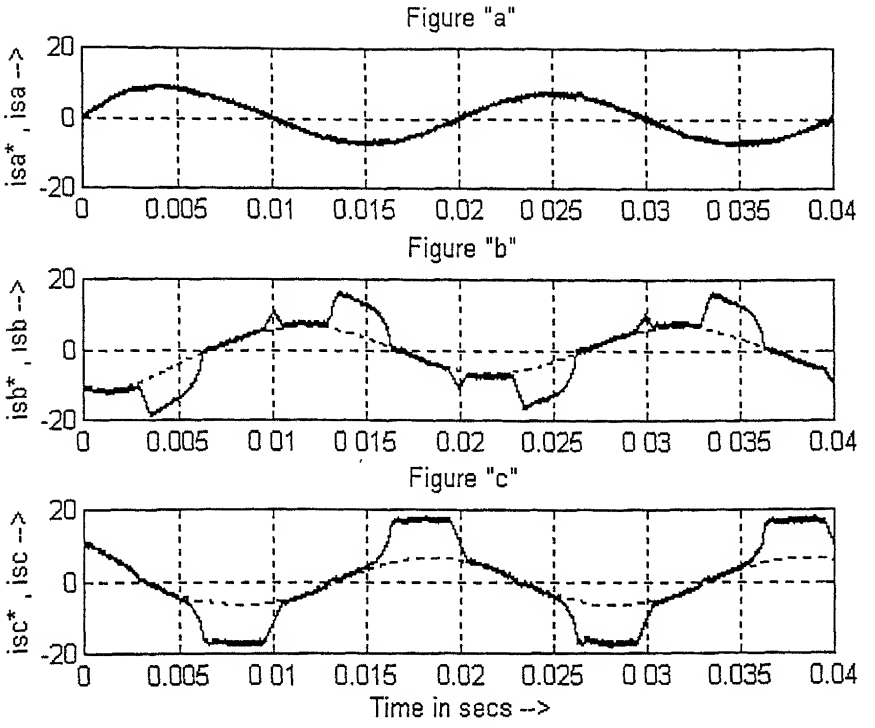

Fig. 4.4 : Results under unbalanced situation.

4.3 Compensation with Three-level Inverter

For high power level applications multi-level inverters have been used, among which three level inverter [7] is the most popular one. The three level inverter configuration used for instantaneous reactive and harmonic power compensation is illustrated in Fig. 4.5. It employs the constant switching frequency technique. Some of the results have already been shown in Chapter 3.

The configuration in Fig. 4.5 shows that four switching devices are used for each phase. Two capacitors are connected with a common point 'n' which makes it possible for three level operation. Thus, each of the three phase output voltages could attain any of the three voltage levels, namely V_{c1}, 0 and $-V_{c2}$. To make it so the inverter has three modes of operations as described below. Only phase-a mode of operation is described as the other two phase operations are quite similar. The description given below is referred to Fig. 4.5.

Mode 1.

In this mode of operation, E_{an} is clamped to V_{c1}.This is achieved by making the top two devices on phase-a ON (k_{a1} =1 and k_{a2} =1) and bottom two devices on phase-a OFF (k_{a3} = 0 and k_{a4} = 0). The phase-a current i_{cma} then flows through the path 'n-V_{c1}-k_{a1}-k_{a2}'. The negative current in this case flows through the diodes connected in anti-parallel with the top two devices.

Mode 2.

The phase output voltage E_{an} becomes zero in this case. This is achieved by switching the four devices in phase-a as follows.

k_{a1} =0, k_{a2} =1, k_{a3} =1 and k_{a4} =0.

This indicates that the middle two devices are made ON and both top and bottom devices are made OFF thereby clamping the output voltage terminal to the neutral point n and thus E_{an} becomes zero. The positive i_{cma} flows through 'n-D_{a1}- k_{a2}' and the negative i_{cma} flows through 'k_{a3}- D_{a2}-n'.

Mode 3.

In this mode of operation the bottom two devices are made ON and the top two devices are made OFF so as to clamp E_{an} to - V_{c2}. The switching conditions are then

k_{a1} =0, k_{a2} =0, k_{a3} =1 and k_{a4} =1.

The specified path for the current in this mode of operation is 'n-V_{c2}-k_{a4}-k_{a3}'. The diodes connected with the bottom two devices are operative for positive i_{cma}.

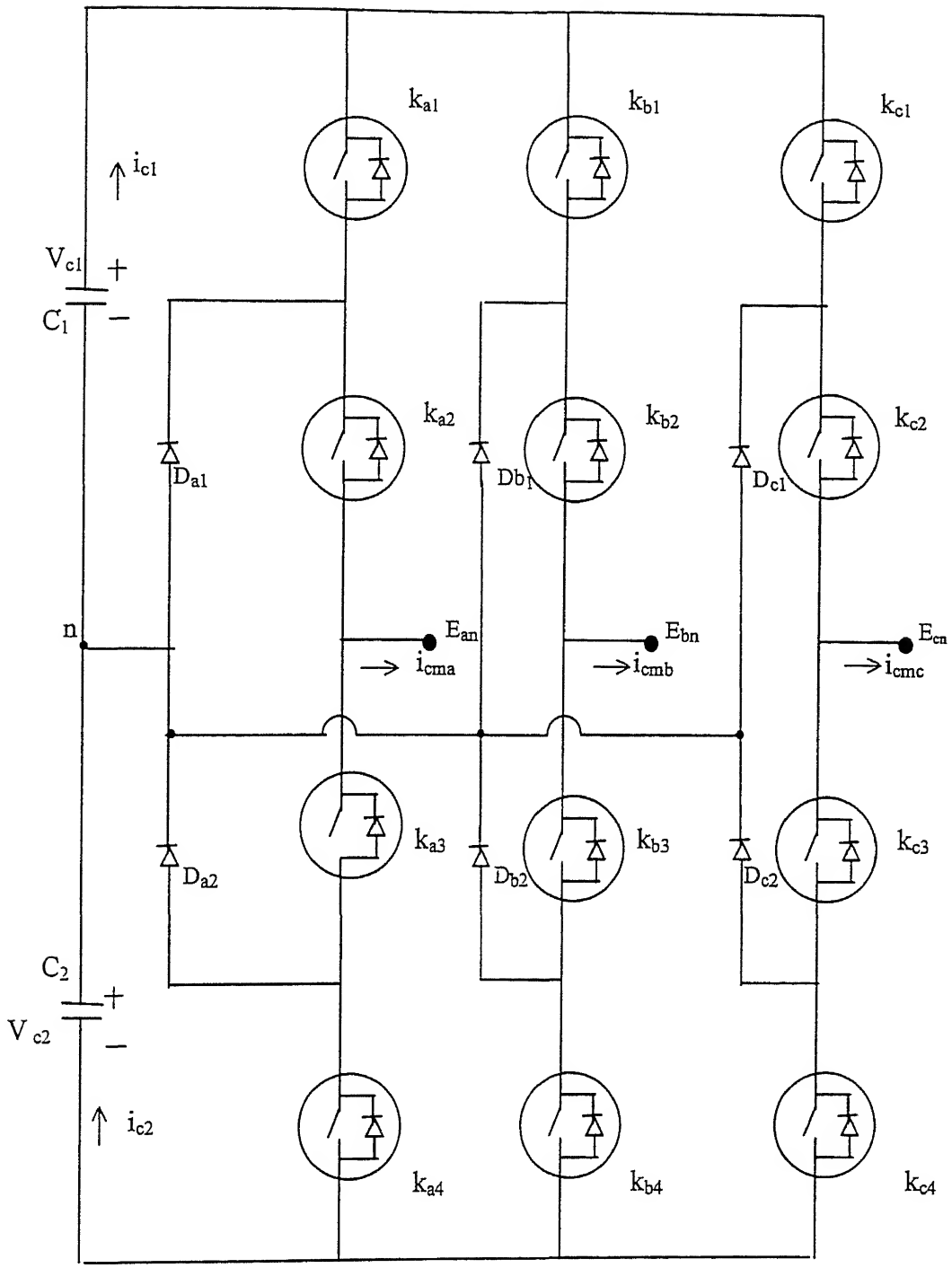

Fig. 4.5 : Configuration of the three level inverter used.

The instantaneous reference currents and the driving signals are obtained as explained in Chapters 2 and 3 respectively. The driving signals (A,B and C) from the current controller gives the information whether the phase currents (i_{cma}, i_{cmb}, and i_{cmc}) are to be increased or decreased. The inverter output voltages (E_{an}, E_{bn}, and E_{cn}) are then clamped to any of the three levels (V_{c1}, 0, and $-V_{c2}$) by selecting the suitable mode of operation for the individual phases. The selection of mode of operation is elaborated for phase-a in two steps as follows.

Step 1 : e_a is positive.

During the positive half cycle of the input system voltage, suppose the current controller's phase-a output signal A changes from 0 to 1 indicating that i_{cma} is to be increased. E_{an} should be more positive than e_a indicating that E_{an} should be clamped to V_{c1} by selecting the Mode 1 operation for phase-a. Also, V_{c1} should be more than the maximum phase-a input system voltage e_a. In this case the capacitor is initially charged to 400 V to satisfy the criteria that $V_{c1} > (e_a)_{max}$.

When A changes from 1 to 0 indicating a need of decrease of current i_{cma} which can then be obtained by clamping E_{an} to a voltage level lower than e_a. Both Mode 2 and Mode 3 operations does make E_{an} lower that e_a as the later is already positive. When e_a is small, by making $E_{an} = 0$ it may not be sufficient to decrease the current. Therefore, from current control point of view E_{an} should be $- V_{c2}$ during small positive values of e_a and E_{an} should be zero during large positive values of e_a.

Step 2 : When e_a is negative.

The situation in this case is similar to the Step 1. When A changes from 1 to 0 indicating that the current i_{cma} is to be decreased, there is no other option but to make E_{an} equal $- V_{c2}$ as e_a is already negative. But when A changes from 0 to 1 and thus i_{cma} is to be increased, E_{an} could then be either zero or V_{c1}. Due to the similar reasons as in Step1, E_{an} should be V_{c1} during small negative values of e_a and zero during large negative values of e_a. Like V_{c1}, V_{c2} is initially charged to 400 V.

The selection of mode of operation, obtained according to step1 and step2, is illustrated in Table I. PS and PB in the table represent positive small and positive big values of e_a. Similarly NS and NB represent negative small and negative big values of e_a. In the table, 1 represents that switching signal A of the current controller is changed from 0 to 1. Similarly, 0 in the table represents that the switching signal A is changed from 1 to 0. The mode of operation is changed according to this table whenever there is a change in the switching signal A from current controller.

Table I : Selection of the mode of operation for phase-a.

e_a / A	NB	NS	PS	PB
1	Mode 2 ($E_{an} = 0$)	Mode 1 ($E_{an} = V_{c1}$)	Mode 1 ($E_{an} = V_{c1}$)	Mode 1 ($E_{an} = V_{c1}$)
0	Mode 3 ($E_{an} = -V_{c2}$)	Mode 3 ($E_{an} = -V_{c2}$)	Mode 3 ($E_{an} = -V_{c2}$)	Mode 2 ($E_{an} = 0$)

The selection of mode of operation could, otherwise, be obtained by defining small and large values of current errors. This is illustrated in Table II. Current error, denoted as Δi_{ca}, is the reference current (i_{ca}^*) minus the actual current (i_{cma}) of the inverter. Hence. positive current error indicates that the current is to be increased and negative current error means that the current is to be decreased. Whenever the switching signal A changes its state requiring a change in the mode of operation, the mode of operation can then be selected according to the Table II. P and B in the table represents positive and negative values of e_a.

Table II : Selection of the mode of operation for phase-a.

Δi_{ca} / e_a	NB	NS	PS	PB
P	Mode 1 ($E_{an} = V_{c1}$)	Mode 2 ($E_{an} = 0$)	Mode 1 ($E_{an} = V_{c1}$)	Mode 1 ($E_{an} = V_{c1}$)
N	Mode 3 ($E_{an} = -V_{c2}$)	Mode 3 ($E_{an} = -V_{c2}$)	Mode 2 ($E_{an} = 0$)	Mode 3 ($E_{an} = -V_{c2}$)

From Tables I and II, it is clear that the boundary between small and large values is to be defined, either for current errors or for input system voltages. Since it is the voltage difference (E_{an} - e_a) which controls the current error, controlling this voltage difference minimises the current error. Table I is dealing with creating voltage differences and suitably selecting the mode of operation. Therefore, Table I is employed for selection of mode of operation of the inverter.

Fig. 4.6 shows the response of the three level inverter, employing Table I to select the mode of operation of the inverter. This is obtained by defining the small and large values of input system voltage. Here, within 7^0 on either side of the zero voltage it treated as small and the rest as large values. It is clear from Fig.4.6 (b) that negative E_{an} appears during positive half cycle of e_a only during the specified region of 7^0. While defining this boundary (7^0) between small and large voltages, it is kept in mind that maximum voltage difference occurs at the boundary and is equal to | V_{c1} + E_m * sin (7^0) |. Where E_m is the maximum phase voltage of the supply system. This maximum voltage difference affects the design of the inductance L_c and the maximum allowable current error.

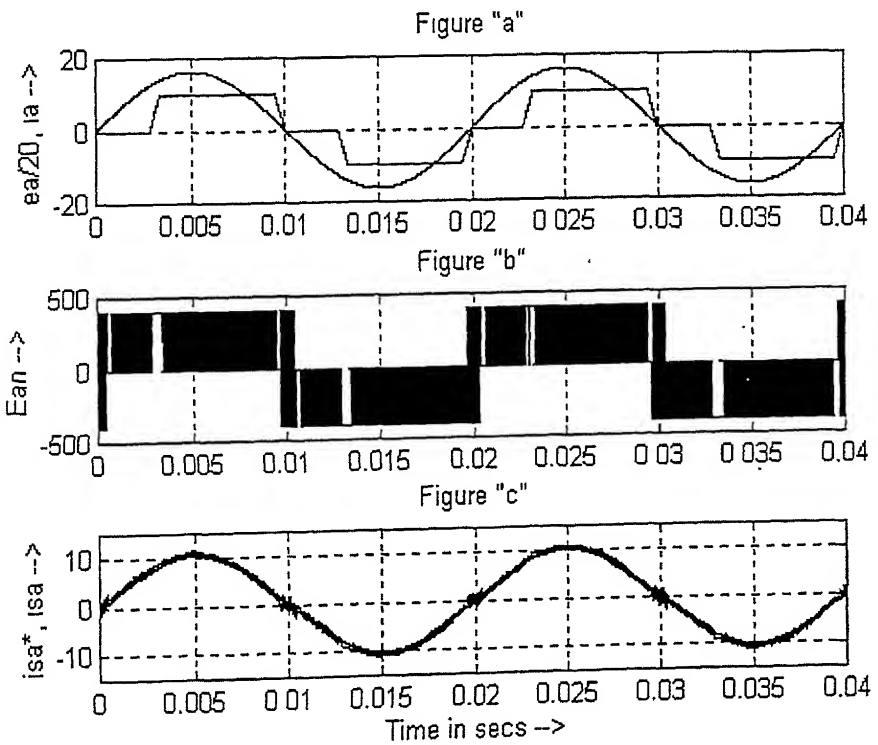

Fig. 4.6 : Output phase voltage wave form of three level inverter.

The following equations are used governing the instantaneous operation of the inverter as a compensator. The phase output voltages of the inverter are.

$$E_{an} = k_{a1} * V_{c1} - k_{a4} * V_{c2}. \quad (4.3.1)$$

$$E_{bn} = k_{b1} * V_{c1} - k_{b4} * V_{c2}. \quad (4.3.2)$$

$$E_{cn} = k_{a1} * V_{c1} - k_{c4} * V_{c2}. \quad (4.3.3)$$

The instantaneous phase currents from the inverters i_{cma}, i_{cmb} and i_{cmc} are then obtained by solving the equations as in (4.2.4) - (4.2.6).

The instantaneous capacitor currents i_{c1} , i_{c2} and hence the capacitor voltages are,

$$i_{c1} = (k_{a1} * i_{cma} + k_{b1} * i_{cmb} + k_{c1} * i_{cmc}). \quad (4.3.4)$$

$$i_{c2} = - (k_{a4} * i_{cma} + k_{b4} * i_{cmb} + k_{c4} * i_{cmc}). \quad (4.3.5)$$

$$V_{c1} = - (1 / C_1) * \int i_{c1} * dt. \quad (4.3.6)$$

$$V_{c2} = - (1 / C_2) * \int i_{c2} * dt. \quad (4.3.7)$$

The results of compensating reactive and harmonic power are obtained for both balanced and unbalanced loads and presented in both cases that follows. It has been assumed that each of the two capacitors are initially charged to 400 V. The value of capacitance for each of the capacitors is 2000 μF and the switching frequency is taken to be 10 kHz. Other parameters remain as in the case of two level inverters.

CASE 1 : (Balanced load condition)

A balanced controlled rectifier load is considered as in CASE 1 of Sec. 4.2. The results obtained are already presented in Figs. 3.7, 3.10, 3.12, 3.18 and 3.19 of Chapter 3. For the sake of clarity the switchings of phase-a (A) over a complete cycle is presented in Fig. 4.7.

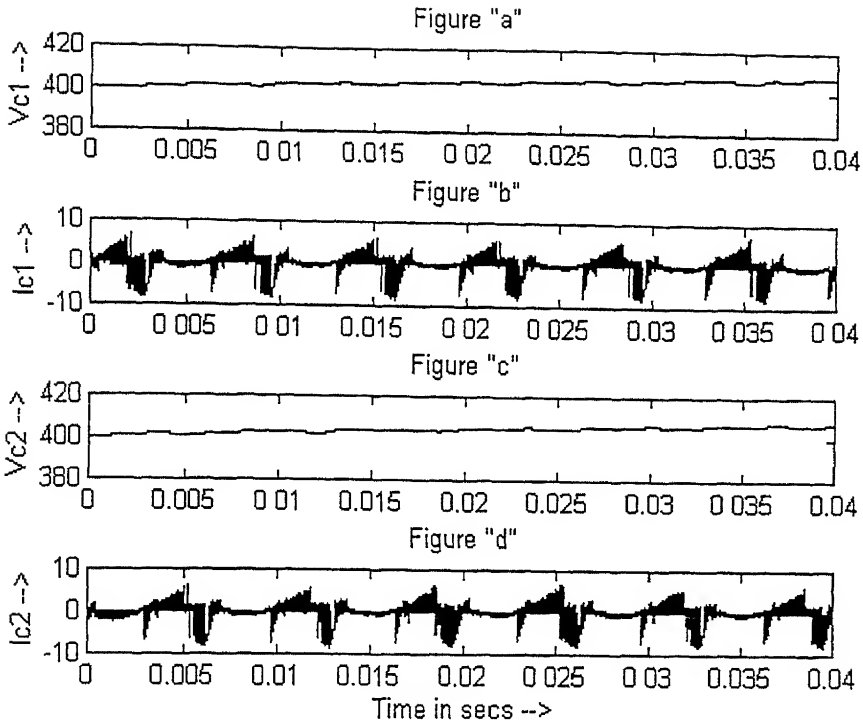

Fig. 4.8 : Capacitor voltages and currents.

CASE 2 : (Unbalanced load condition)

The same unbalanced load as taken in CASE 2 of two level inverter is considered. Thus for the load currents, Fig. 4.3 is to be referred. Fig. 4.9 shows each phase inverter output currents (i_{cma},i_{cmb} and i_{cmc}) and the corresponding phase source currents (i_{sa}, i_{sb} and i_{sc}). The inverter output phase-a current is different from the other two so as to make the source phase currents identical in shape and free from harmonics. It is prominent from the figure that 0.01s is taken for getting proper compensation objectives. This is because of the moving averaging technique used as explained in Chapter 2. It is clear from the figure that the compensator using the three level inverter works under unbalanced cases also.

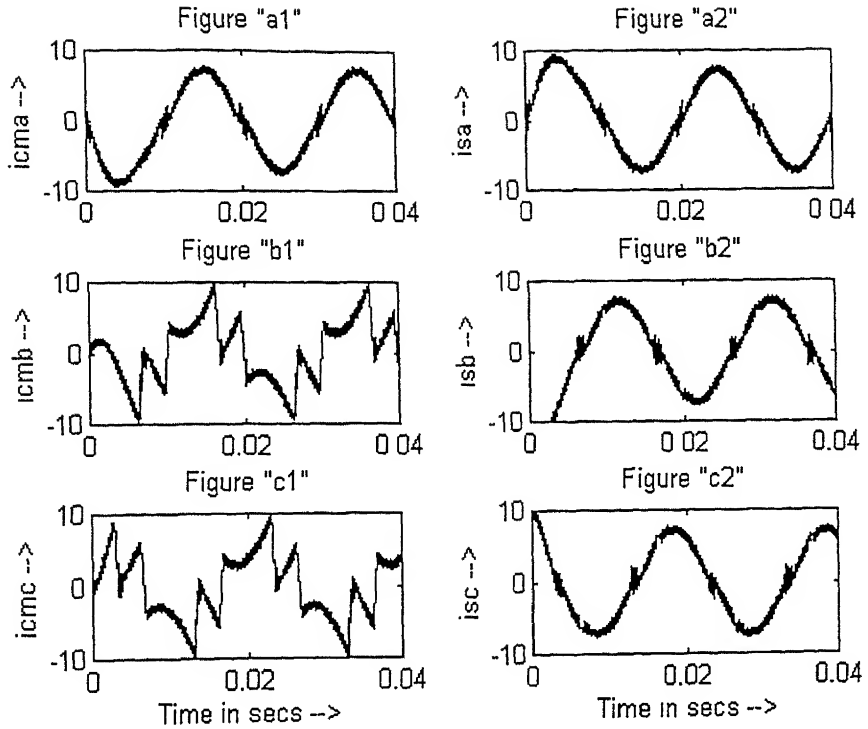

Fig. 4.9 : Inverter currents and Source currents under unbalanced conditions.

Figs. 4.10 and 4.11 reveals the importance of the constant switching frequency current control technique under unbalanced load conditions. Fig. 4.10 shows each phase driving or switching signals (A, B and C) from the current controller for the first quarter cycle (0-0.005s) of input system voltage. Similarly Fig. 4.11 illustrates the driving signals A, B and C for the next quarter cycle (0.005s - 0.01s). It is quite clear that the number of switchings that take place in each of the phases remain constant throughout the cycle, thereby, making the Constant Switching Frequency Technique suitable for the compensator even under unbalanced load conditions.

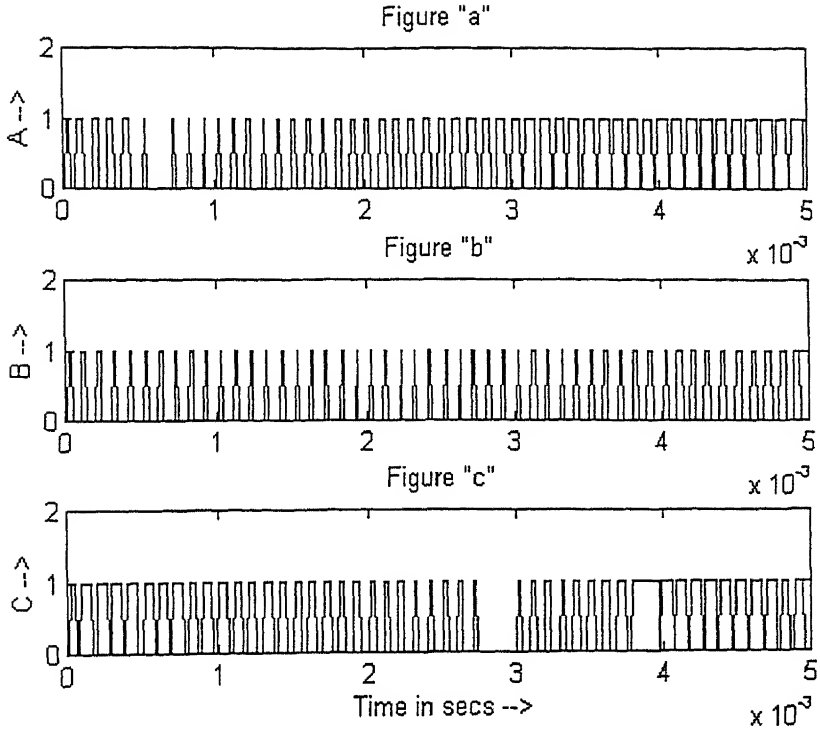

Fig. 4.10 : Switching Signals for a quarter cycle.

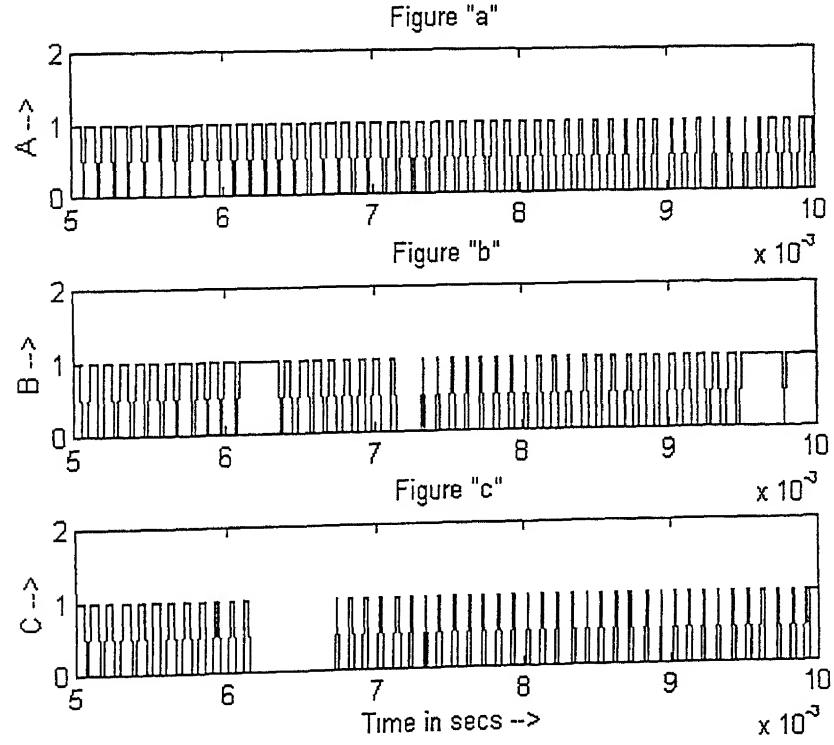

Fig. 4.11 : Switching Signals for next quarter cycle.

Fig. 4.12 illustrates the fluctuation of voltage across the capacitors. Both V_{c1} and V_{c2} are found to be increasing and hence needs to be controlled.

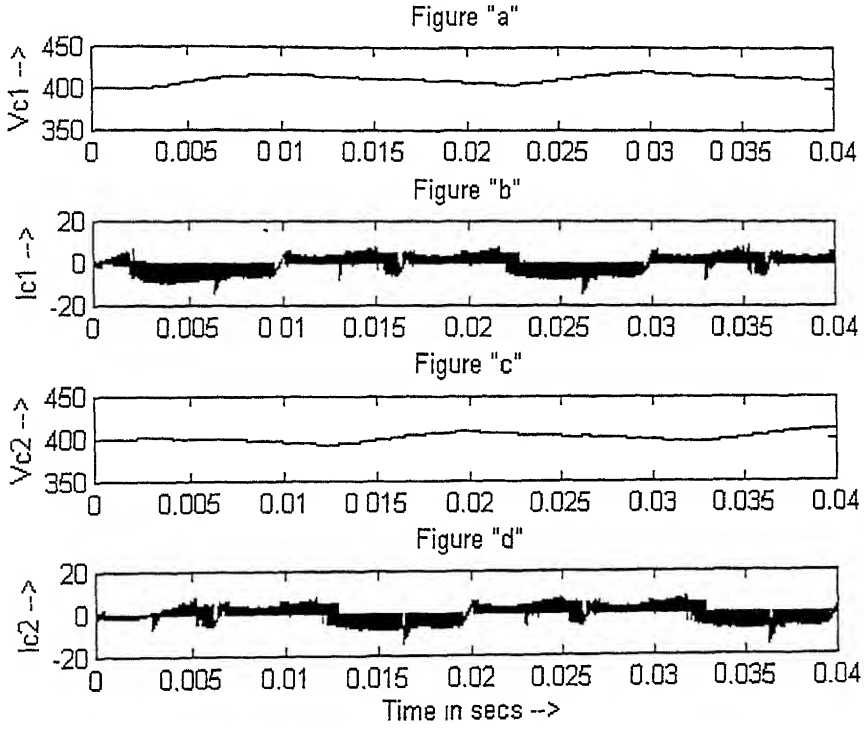

Fig. 4.12 : Voltage across and Current through both of the capacitors.

Finally the effectiveness of the compensation under unbalanced load conditions is shown in Fig. 4.13. This figure illustrates the harmonic spectrum of the source current of phase-a after compensating reactive and harmonic powers. The top figure is the phase-a source current which is the last cycle of i_{sa} shown in subfigure "a2" of Fig. 4.9. The bottom figure illustrates the harmonic spectrum of phase-a source current. It is clear from the figure that the harmonic frequency components are quite small as compared to the fundamental component, thereby, making the compensation effective.

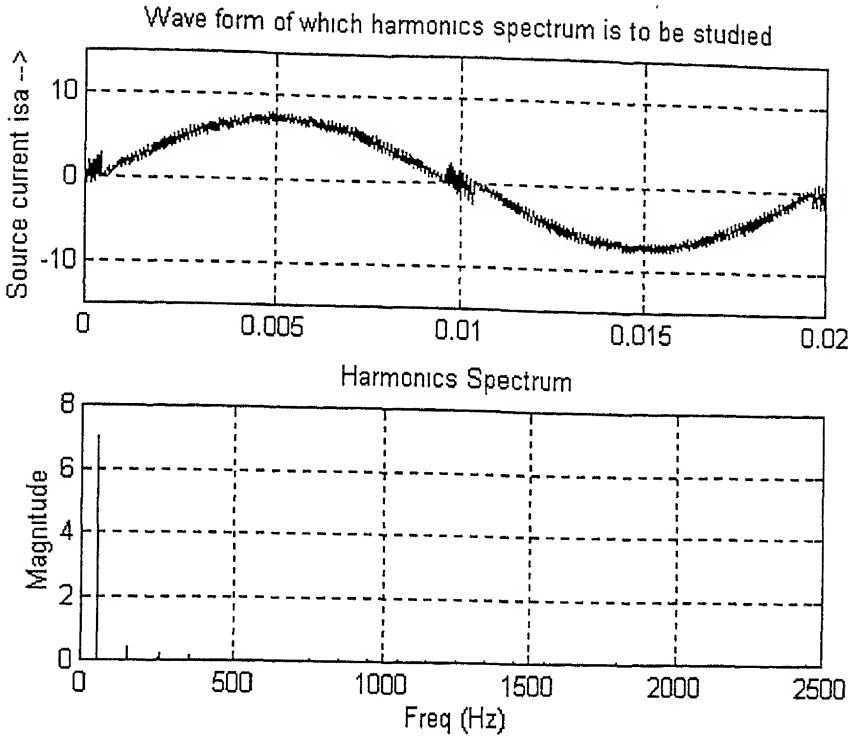

Fig. 4.13 : Harmonic Spectrum of the compensated Source Current (i_{sa}).

4.4 Compensation with Five-level Inverter

The three level operation is extended to five level operation and instantaneous compensation is obtained using the five level inverter working at constant switching frequency. Thus the compensator is suitable for higher power levels. The configuration of the five level inverter is shown in Fig. 4.14, which is quite similar to that of the three level inverter except that the number of components used in this case are more for making it suitable for a five level operation. It employs four capacitors at its input having a neutral point 'n'. This ensures in providing two levels in both positive and negative voltages and also a zero voltage level. It is, therefore, called five level inverter.

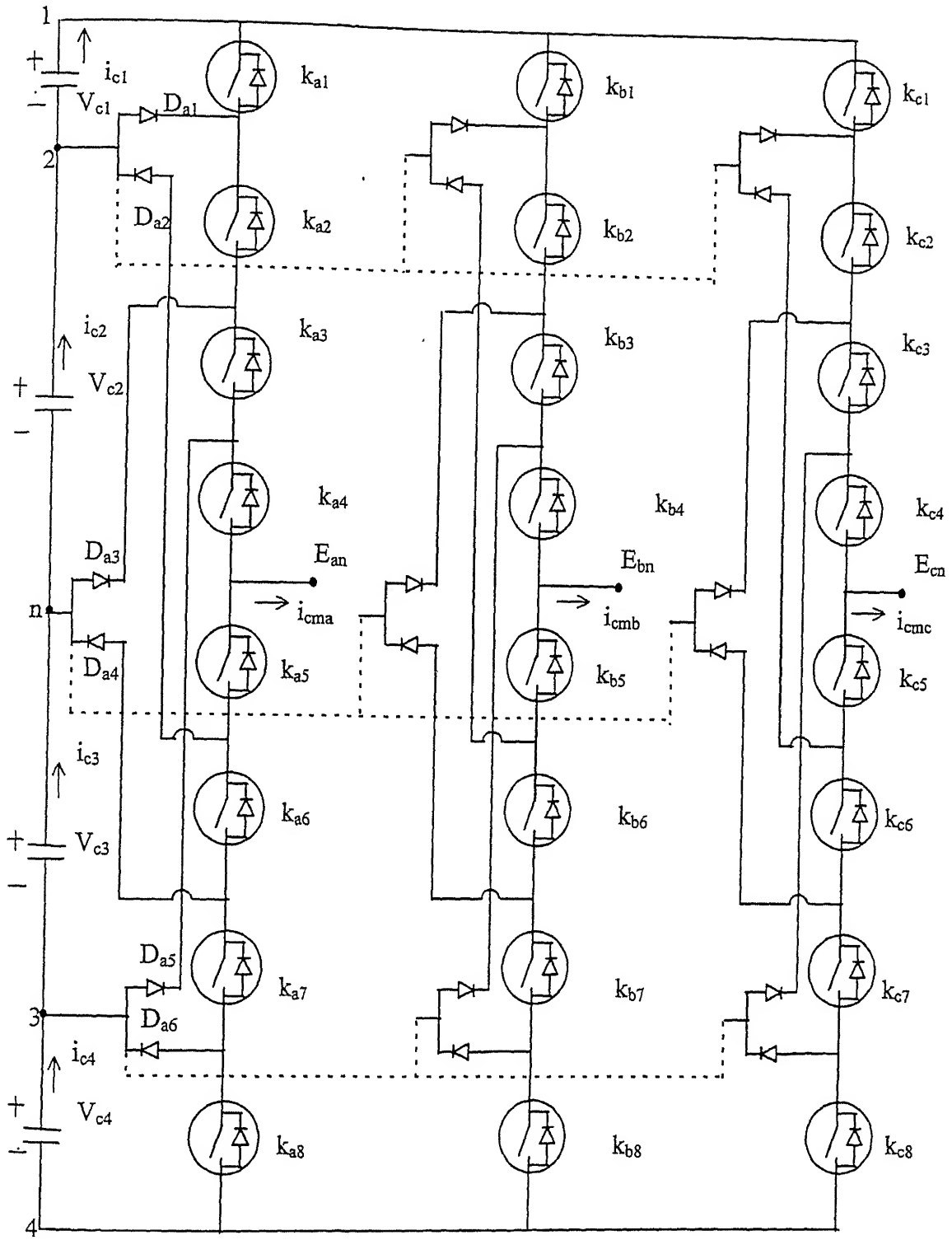

Fig. 4.14 : Configuration of the five level inverter used.

The different modes of operation for phase-a to provide a five level operation are shown in Table III. The other two phase operations are similar to phase-a operation.

In Table III, switching conditions for different modes are shown in the third column, each row of which contains eight binary numbers (either 1 or 0) separated by commas. The first number in the row refers to the switching condition of the device k_{a1} in Fig. 4.14. Similarly the second number for k_{a2}, third for k_{a3} and so on. Thus switching conditions of all the eight devices connected in phase-a are clear from the table. In each row, showing the switching conditions, 1s and 0s indicate that the corresponding devices are turned ON and OFF respectively. For example in Model of operation '1,1,1,1,0,0,0,0' in the table represents that the devices k_{a1}, k_{a2}, k_{a3} and k_{a4} are turned ON while k_{a5}, k_{a6}, $k_{a7}$and k_{a8} are turned OFF.

In the Table III, paths for the current i_{cma} are specified for each mode of operation. Whenever k_{a1} is specified in the path, it means that the device k_{a1} in Fig. 4.14 is conducting. And d_{a1} shown in the path means that the diode connected in anti-parallel with the device k_{a1} in Fig. 4.14, is conducting. Similar is the case with other notations (k_{a2} - k_{a8} and d_{a2} - d_{a8}) used in this table.

Table III : Modes of operation for 'phase-a' of the inverter.

Operating Mode	Output 'E_{an}'	Switching conditions	Path for +ve 'i_{cma}'	Path for -ve 'i_{cma}'
Mode 1	($V_{c1} + V_{c2}$)	1, 1, 1, 1, 0. 0, 0, 0	n-1-k_{a1}-k_{a2}-k_{a3}-k_{a4}	d_{a4}-d_{a3}-d_{a2}-d_{a1}-1-n
Mode 2	V_{c2}	0, 1, 1, 1, 1, 0, 0, 0	n-2-D_{a1}-k_{a2}-k_{a3}-k_{a4}	k_{a5}-D_{a2}-2-n
Mode 3	0	0, 0, 1, 1, 1, 1, 0, 0	n-D_{a3}-k_{a3}-k_{a4}	k_{a5}-k_{a6}-D_{a4}-n
Mode 4	- V_{c3}	0, 0, 0, 1, 1, 1, 1, 0	n-3-D_{a5}-k_{a4}	k_{a5}-k_{a6}-k_{a7}-D_{a6}-n
Mode 5	- ($V_{c3} + V_{c4}$)	0, 0, 0, 0, 1, 1, 1, 1	n-4-d_{a8}-d_{a7}-d_{a6}-d_{a5}	k_{a5}-k_{a6}-k_{a7}-k_{a8}-4-n

Selecting the mode of operation at a particular instant is now a difficult task as the number of modes of operation is more. Selection of the operating mode for phase-a is shown in Table IV. Suppose the phase-a system voltage e_a is positive and controller output A is 1, then current can be increased by clamping E_{an} to a positive voltage, which can then be obtained by either Mode 1 or Mode 2. Which mode to be applied depends on the positive value of e_a as E_{an} is to be more than e_a for increasing the current. Similarly if A is 0 during positive half cycle of e_a, phase-a current can then be decreased by any of the three modes namely Mode3, Mode 4 and Mode5. Selection of the mode of operation then depends on how much positive e_a is. Thus the selection is then performed by defining different levels of voltage e_a. This is described as follows.

e_a is positive small (PS), when $0 < e_a \leq E_m * \text{Sin}(\theta_1)$.

e_a is positive medium (PM), when $E_m * \text{Sin}(\theta_1) < e_a \leq E_m * \text{Sin}(\theta_2)$.

e_a is positive big (PB), when $e_a > E_m * \text{Sin}(\theta_2)$.

Similarly,

e_a is negative small (NS), when $0 > e_a \geq -E_m * \text{Sin}(\theta_1)$.

e_a is negative medium (NM), when $- E_m * \sin(\theta_1) > e_a \geq - E_m * \sin(\theta_2)$.

e_a is negative big (NB), when $e_a > - E_m * \sin(\theta_2)$.

Where E_m is the maximum value of system phase voltage. θ_1 and θ_2 is to be decided to achieve proper current control. For example when e_a is PM and A is 1 then Mode2 is selected as shown in Table IV, thereby, E_{an} is V_{c1}. To increase the current E_{an} should be greater than e_a, thus θ_2 should be decided such that $E_m * \sin(\theta_2) < V_{c1}$. However there is no such condition for deciding θ_1. Here, while selecting the mode of operation Fuzzy Logic could be applied, taking fuzzy boundaries instead of crisp boundaries, for defining ranges of small, medium and big voltage (e_a).

For this five level operation of inverter, θ_1 and θ_2 are chosen as 9^0 and 27^0 respectively. The capacitors are assumed to have initial voltage of 200 volts each and the capacitance of each of them is taken to be 2000 μF. Selection of phase-a mode of operation are shown in Table IV. Selection of the other two phase operations are identical to this.

Table IV : Selection of the mode of operation for phase-a.

A \ e_a	NB	NM	NS	ZERO	PS	PM	PB
1	Mode 3	Mode 2	Mode 1	Mode 2	Mode 2	Mode 2	Mode 1
0	Mode 5	Mode 4	Mode 4	Mode 4	Mode 5	Mode 4	Mode 3

The working of the five level inverter, used as instantaneous reactive and harmonic power compensation, is described as follows.

After the switching signals obtained from the current controller, the mode of operation for all the three phases are decided according to the logic given in Table IV. Once the modes of operations are decided, the switching condition (ON or OFF) of all the devices

are then derived as explained in Table III, thereby fixing the values of the inverter phase output voltages. The phase currents i_{cma}, i_{cmb} and i_{cmc} are obtained from Eqns.(4.2.4) - (4.2.6).Then the capacitor currents and hence the capacitor voltages are,

$$i_{c1} = (k_{a1} * i_{cma} + k_{b1} * i_{cmb} + k_{c1} * i_{cmc}). \quad (4.4.1)$$

$$i_{c2} = (k_{a2} * i_{cma} + k_{b2} * i_{cmb} + k_{c2} * i_{cmc}). \quad (4.4.2)$$

$$i_{c3} = - (k_{a7} * i_{cma} + k_{b7} * i_{cmb} + k_{c7} * i_{cmc}). \quad (4.4.3)$$

$$i_{c4} = - (k_{a8} * i_{cma} + k_{b8} * i_{cmb} + k_{c8} * i_{cmc}). \quad (4.4.4)$$

$$V_{c1} = - (1 / C_1) * \int i_{c1} * dt. \quad (4.4.5)$$

$$V_{c2} = - (1 / C_2) * \int i_{c2} * dt. \quad (4.4.6)$$

$$V_{c3} = - (1 / C_3) * \int i_{c3} * dt. \quad (4.4.7)$$

$$V_{c4} = - (1 / C_4) * \int i_{c4} * dt. \quad (4.4:8)$$

The results of compensation are obtained for both balanced and unbalanced load conditions and illustrated as follows.

CASE 1 : (balanced load condition)

The balanced load considered is same as that in two level and three level inverter cases, hence not shown again. Fig. 4.15 shows i_{cma}, E_{an} and switching signal A for one half cycles. Fig. 4.16 shows the compensated phase-a source current i_{sa} and its harmonic spectrum. The results shown reveal that, five level inverter offers best compensation and it works at constant switching frequency as well.

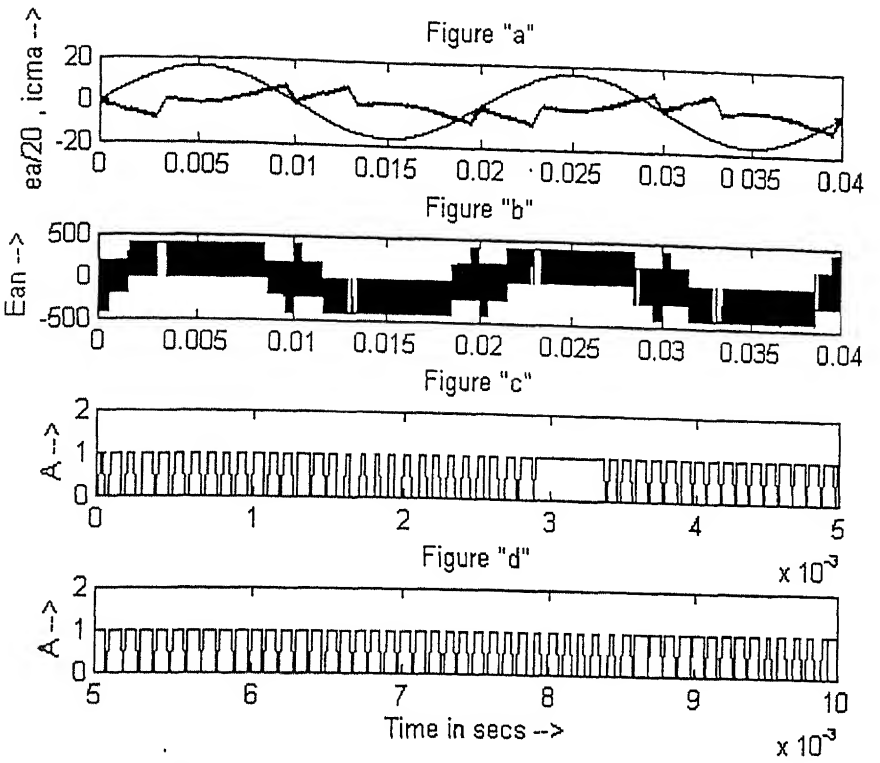

Fig. 4.15 : Results in case of balanced loads.

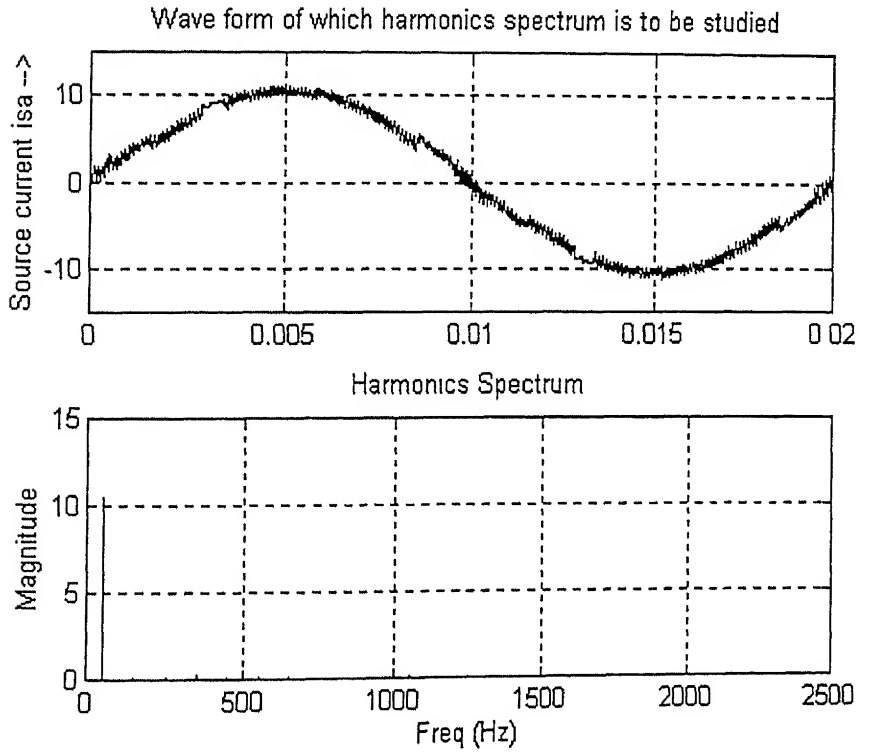

Fig. 4.16 : Harmonic Spectrum of phase-a compensated Source Current.

Fig. 4.17 shows the fluctuation of each of the capacitor voltages. Like the case with three level inverter already discussed, the capacitor voltages are increasing continuously. The factors, causing the increasing in capacitor voltages, are discussed in Chapter 5.

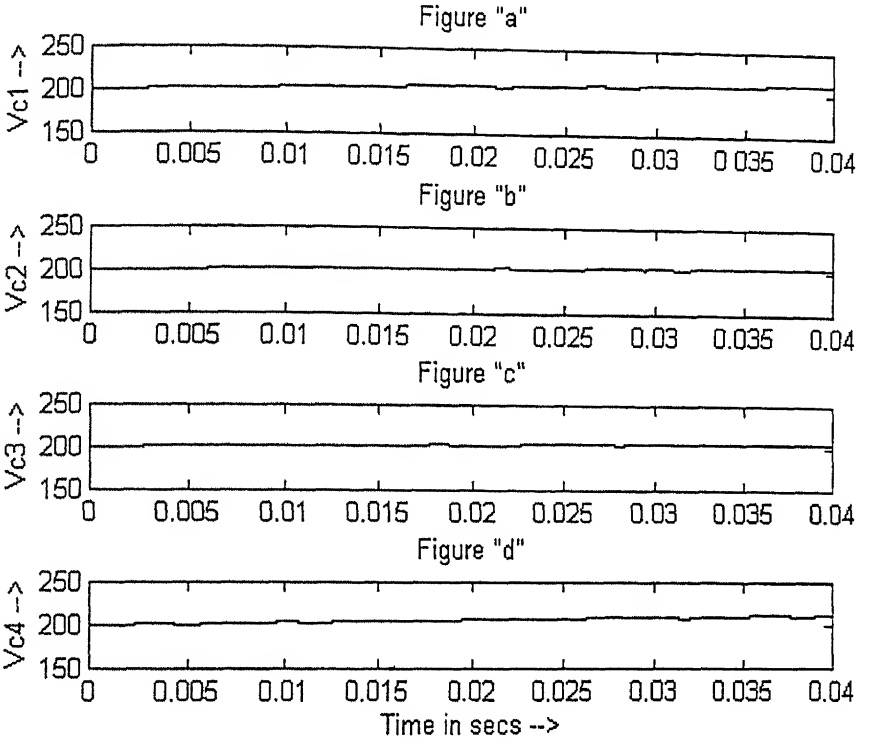

Fig. 4.17 : Capacitor Voltages.

CASE 2 : (unbalanced load condition)

Unbalanced situation is created as explained in Sec. 2 of this chapter and compensation is obtained with this five level inverter operating at constant switching frequency. The results of compensation are shown in Figs. 4.18 and 4.19. It is clear that, it works successfully under unbalanced load conditions. Harmonic spectrum of phase-a compensated source current, is illustrated in Fig. 4.19. This compensator provides excellent compensation characteristics even under unbalanced situation, as it is clear from the results shown.

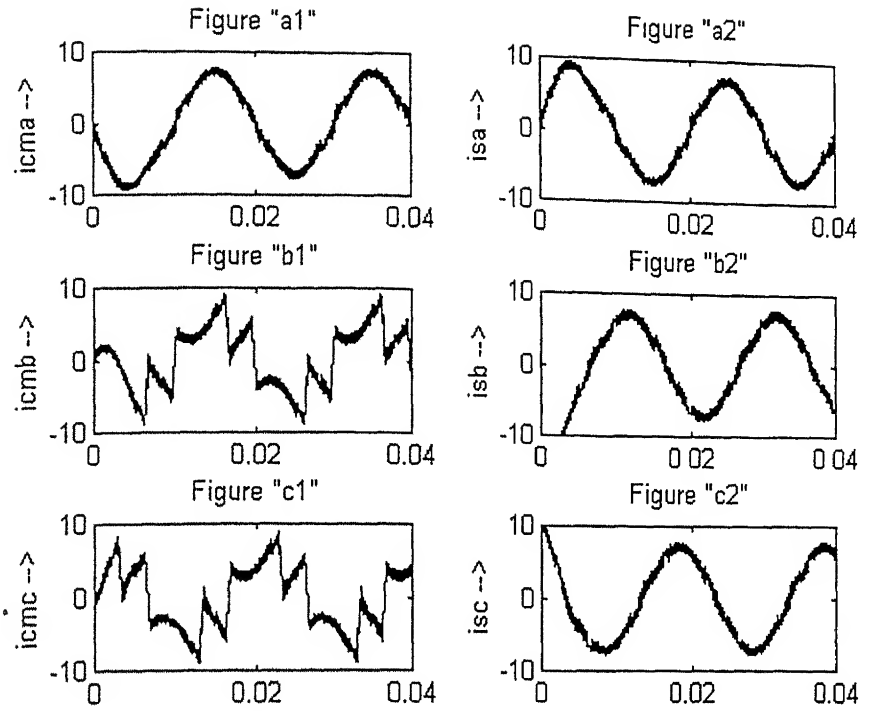

Fig. 4.18 : Inverter currents and Source currents under unbalanced conditions.

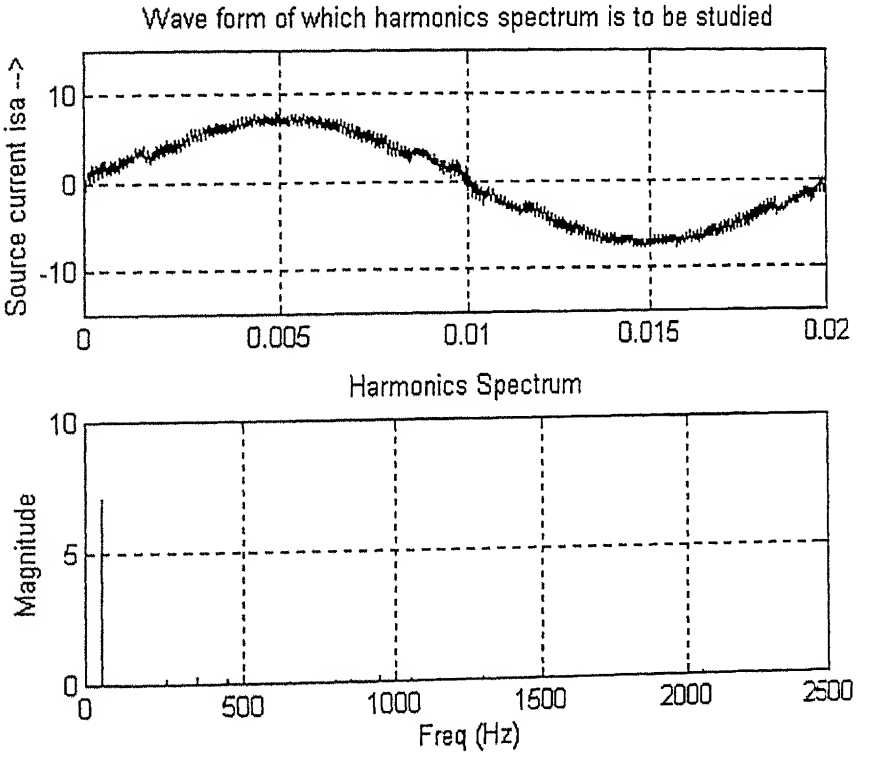

Fig. 4.19 : Harmonic Spectrum of compensated phase-a source current.

The switchings that take place for all the three phases, are shown in Fig. 4.20 over a half cycle, indicate that the inverter operates at constant switching frequency.

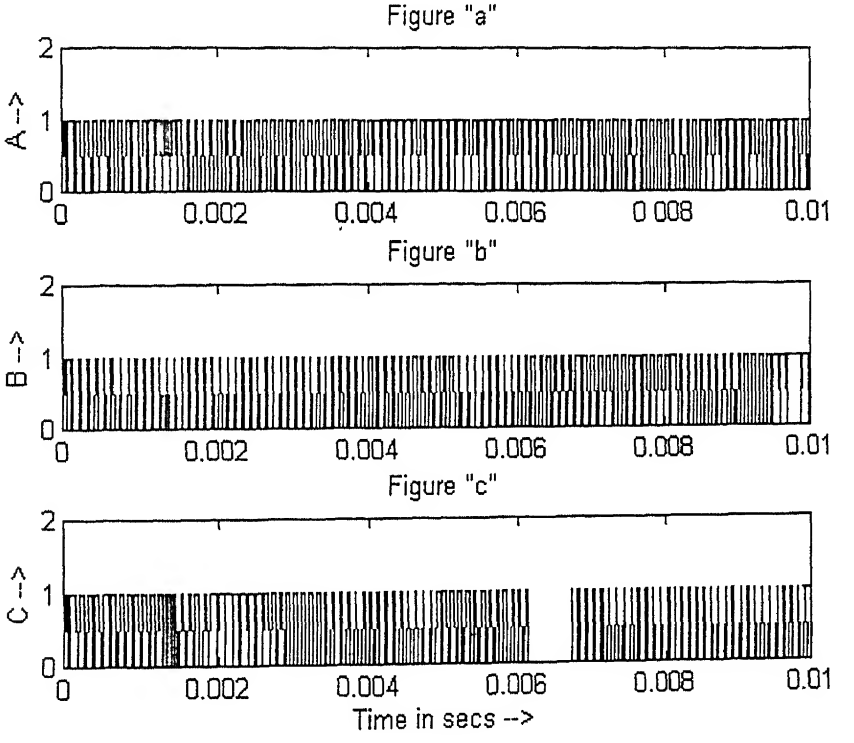

Fig. 4.20 : Switching signals for each phase, over a period of half cycle.

4.5 Conclusion

It has been shown in this chapter that constant switching frequency technique works successfully for the inverters to compensate instantaneous reactive and harmonic powers. Two level configuration when used for compensation, fails under unbalanced load conditions, as evident from Sec. 2 of this chapter. Three level and five level configurations offers satisfactory compensation characteristics even under unbalanced situations. Though five level configuration provide best results among the three configurations, there is not much difference between the results of three level and five level cases. Therefore, from compensation point of view, it may not be advisable to use five level inverter, employing more number of devices and making the system more complicated. Fuzzy Logic Controller may be a suitable option for the five level inverter.

Voltage Control aspect is not included for the configurations used in this chapter. Therefore, voltage of each capacitors is diverging from their initial values even if the system is loss less (assumed for all the inverters in this chapter). Adding the voltage control feature to each, will make the compensation successful at steady state. It will be clear in Chapter 5 that, these configurations require special modulation techniques, for selecting the mode of operation.

All the configurations of inverter discussed in this chapter, shape the inverter output phase currents with the help of common input capacitors. So any fault occurring in any of the phases may affect the other phase operations, as happening in case of two level inverter. A simple approach is to handle the phase reference currents separately. This requires three inverters to take care of each phase reference currents separately, thus making the operation simpler and suitable for any adverse situations by providing independent compensations for each phase. This aspect is explored and instantaneous reactive and harmonic power compensation is obtained, using three single phase inverters, connected in a Wye fashion. Inverter losses, not considered so far, are considered for this case and then compensation is obtained with voltage control feature added for the inverter. The configuration of this inverter makes it suitable for three level operation and provides the same kind of compensation characteristics as in Sec. 4.3 of this chapter, without requiring any special modulation technique. The details of this, are presented in Chapter 5 that follows.

Chapter 5

COMPENSATION WITH THREE SINGLE-PHASE THREE-LEVEL INVERTER

5.1 Introduction

The configurations presented in Chapter 4 are able to operate at constant switching frequency with reasonable compensation characteristics. But the two Level Inverter fail to operate under unbalanced load conditions, as seen in Sec. 4.2. Also, three and five level configuration used for compensation and discussed in Secs. 4.3 and 4.4 respectively, show that the dc capacitor voltages increase/decrease continuously and thus will fail in steady state. It is, therefore, required to analyse the effect of compensating each of the power components($\tilde{p}$,$\tilde{q}$ and $\bar{q}$) on capacitor voltages. In [2], it is explained that $\tilde{p}$ represents the energy per second that is being transported from source to load or vice-versa at any time, and the reactive power $q = \tilde{q} + \bar{q}$ does not contribute for the energy transport. Therefore, it is the power component $\tilde{p}$ but not q which cause this continuous increase/decrease in capacitor voltages. This is more clear in [3] which employs a separate voltage control loop to compensate the effect of $\tilde{p}$ on the capacitor voltage. There should not be any steady increase in capacitor voltages if the power component q alone is compensated. When the compensator compensates the power components ($\tilde{p}$ and q) there

is an steady increase/decrease of capacitor voltages from cycle to cycle as may be noted from Figs.4.8 and 4.17 for three level and five level inverters in Chapter 4. Therefore, there is a need to know whether the capacitor voltage variation is caused by compensating $\tilde{p}$ and / or q. Thus, to start with, q alone is compensated with the three level inverter as in Sec. 4.3 of Chapter 4. The capacitor voltages are determined and shown in Fig. 5.1. Comparing this figure with Fig.4.8, it is clear that compensating q alone also cause this variation, although strictly speaking it should not result in capacitor voltage variation.

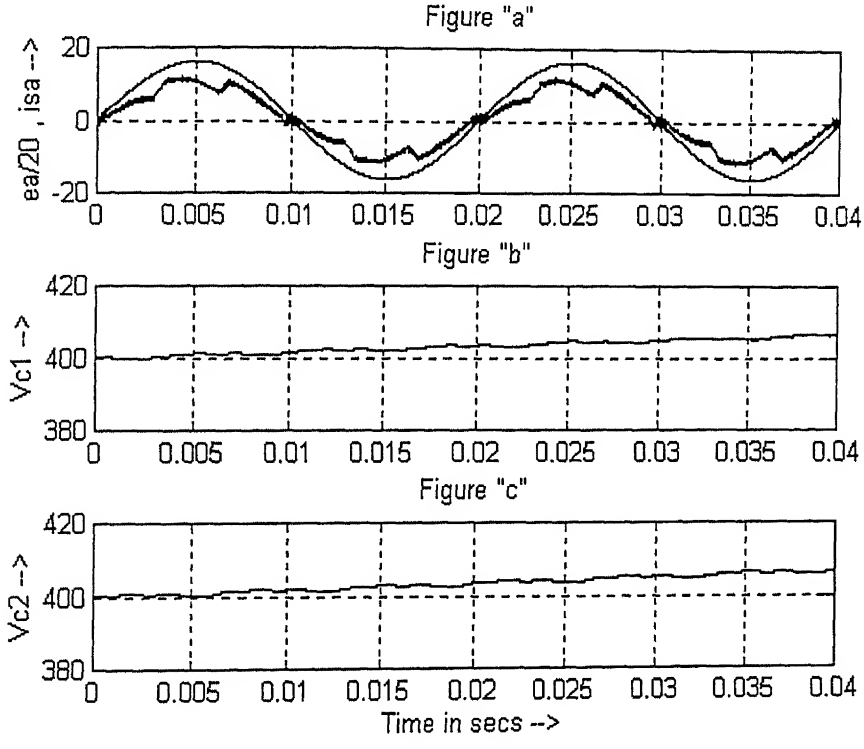

Fig. 5.1 : Capacitor voltages when only reactive power q is compensated.

As the power component q does not contribute to any instantaneous energy storage [2], it is now clear that proper care is to be taken while selecting the mode of operation for the inverter. In other words additional voltage control aspect is to be considered for selecting the mode of operation, which makes the system more complicated [9]. This is the drawback of the multi-level configurations, presented in Chapter 4. It would be better if the three phases are controlled independently. This, therefore, requires three capacitors for the three phases. This gives rise to three single-phase inverter configurations for the three phases. This is proved to be better than the three level configuration used in

Chapter 4 except that it uses one more capacitor. The compensation is obtained with this configuration and the results are shown in this chapter. Switching losses are also considered and closed-loop operation is performed to compensate these losses.

5.2 Configuration of the Three-level Inverter

The configuration of the inverter using three individual inverters for independent operation of phases is shown in Fig. 5.2. This configuration employs four switching devices and one capacitor per phase. When compared with the three level configuration as in Chapter 4, the number of devices remains the same while the number of capacitors are increased by one. R_c represents both internal resistance of the inductor L_c and the equivalent resistance causing switching losses in each phase.

The inverter is essentially a three phase inverter employing three identical inverters to take care of phases independently. These three individual inverters are connected in Wye configuration with a common point as the neutral. This configuration makes it possible for a three- phase three level inverter. For example, making k_{a1}, k_{a2} ON and k_{a3}, k_{a4} OFF, the phase-a output voltage E_{an} is clamped to + V_{c1}. Similarly to get - V_{c1} , just the switching conditions are reversed. To get a zero voltage at phase-a of the inverter outputs, k_{a1}, k_{a3} are made ON and k_{a2}, k_{a4} are made OFF. Similar is the case with other phases. This gives rise to the three phase and three Level operation of the inverter.

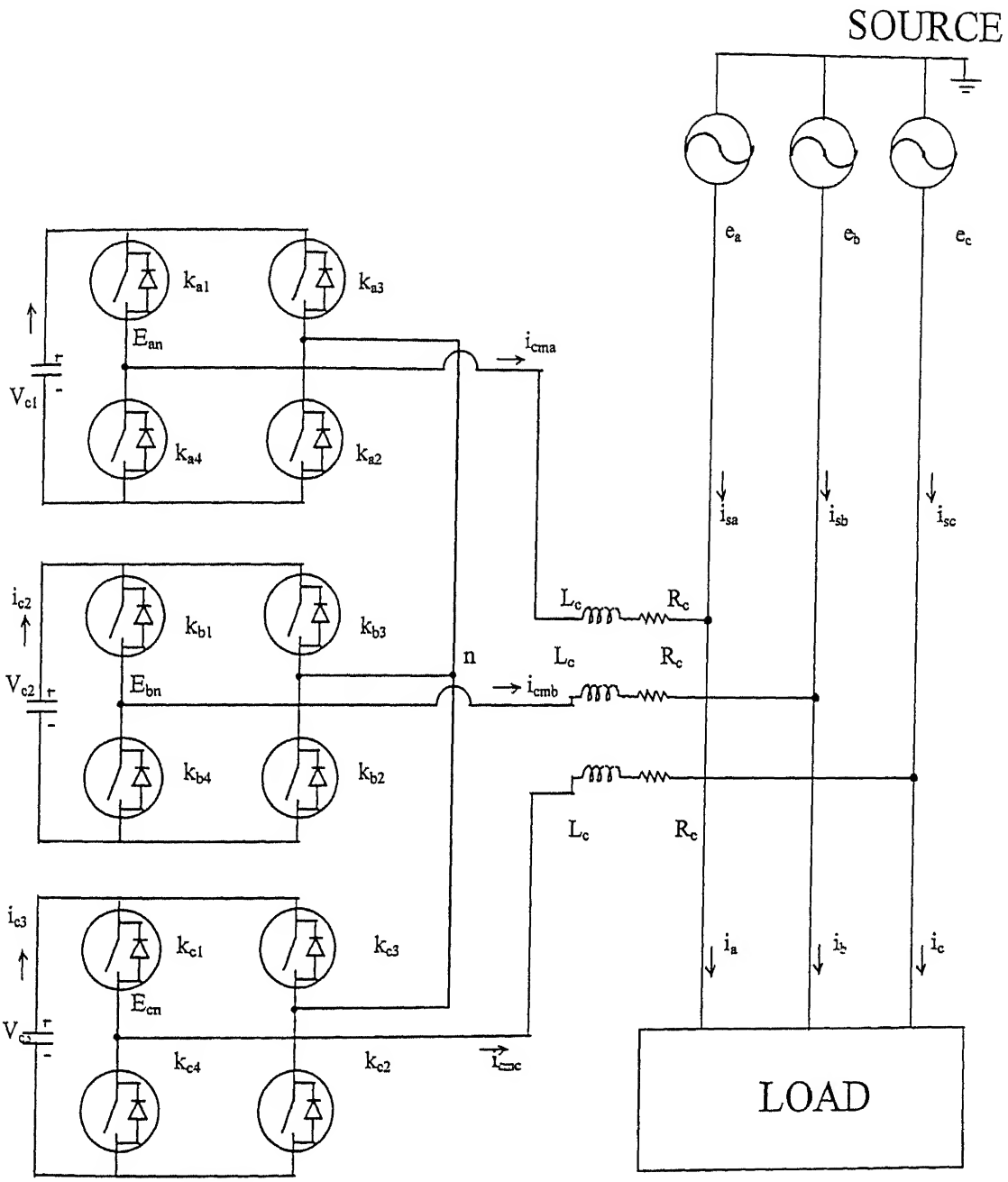

Fig. 5.2 : Configuration of the inverter.

5.3 Compensator System with the Three-level Inverter

Three level operation is performed with the inverter shown in Fig. 5.2, and instantaneous reactive and harmonic power compensation is obtained. The selection of the mode of operation for the inverter is performed in the same way as discussed in Sec. 4.3 of Chapter 4.In Sec. 5.3.1, the system is assumed to be loss-less ($R_c = 0$) and the conditions are the same as the case of three level inverter in Sec. 4.3 of Chapter 4. The results obtained with these two configurations of three level inverters are especially from voltage control point of view.

In Sec. 5.3.2, a rectifier load with zero delay angle is considered. Compensation is then obtained by taking the switching losses also into account (Rc taken as 2 Ω). The results are shown for both cases, i.e. without voltage control loop and with voltage control loop.

5.3.1 Open-loop Operation

The load conditions and the other parameters are taken to be the same as CASE 1 in Sec. 4.3 of Chapter 4. As mentioned already, the selection of modes of operation also remain the same as before. The power component $q = \tilde{q} + \bar{q}$ alone is compensated using this inverter configuration (Fig. 5.2) with three level operation. The capacitor voltages are then found as in Fig. 5.3.

The sub-figure a of Fig. 5.3 shows that the inverter is operating at three level. The other three sub-figures show the capacitor voltages. It is evident from these subfigures a, b and c that there is no steady increase or decrease in any of the capacitor voltages. Comparing these results with that shown in Fig. 5.1, is clear that this configuration does not need voltage control features while selecting the modes of operation for the inverter. Therefore, this configuration will provide better current control capability as we are free to choose the mode of operation. The situation is complicated when both voltage control and current control are combined together for the three level inverter described in Sec 4.3 of Chapter 4 [9].

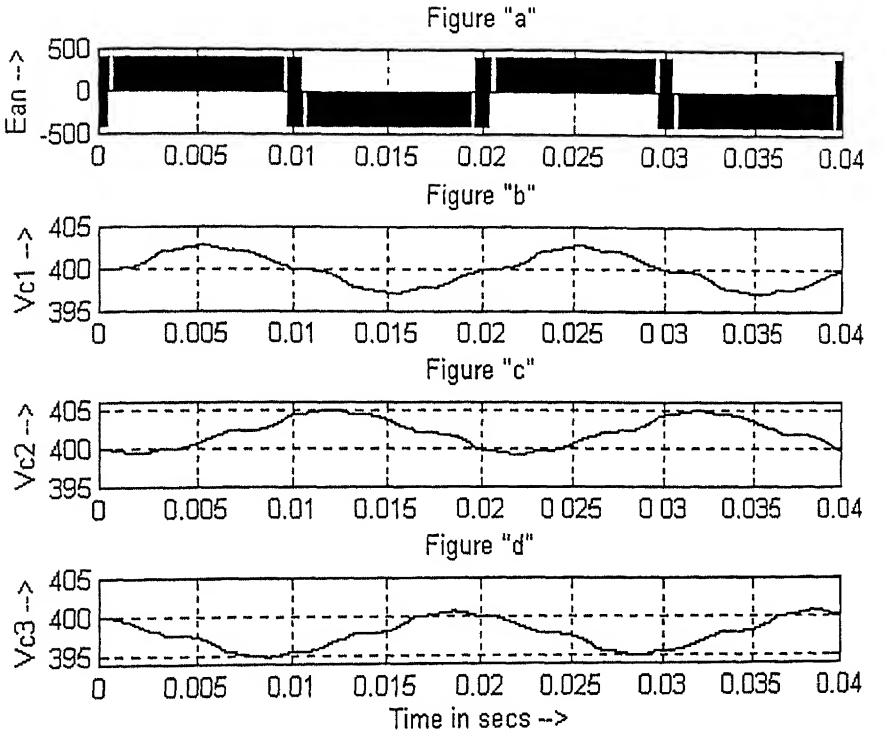

Fig. 5.3 : Capacitor voltages when only reactive power (q) is compensated.

Fig. 5.4 shows the capacitor voltages for five cycles (0s to 0.1s) of input system voltage. It is clear, that the configuration is suitable for steady state operation without controlling the voltage provided the system is loss-less and $\tilde{p}$ is not compensated.

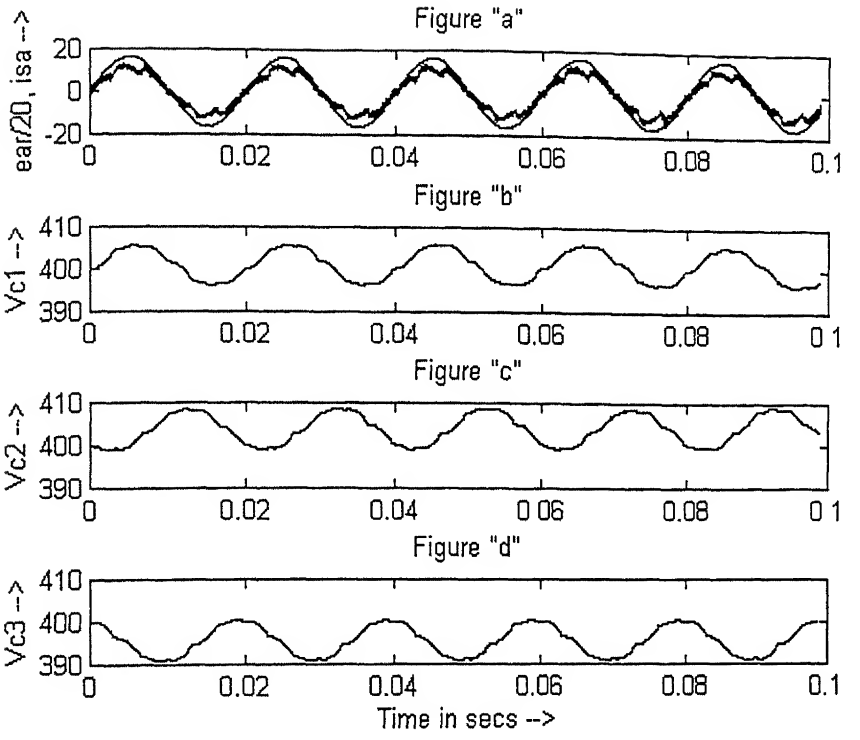

Fig. 5.4 : Capacitor voltages(Over a period of five cycles of input system voltage) when only reactive power (q) is compensated.

Fig. 5.5 shows the capacitor voltages, when only the power component $p^{\sim}$ is compensated. The source i_{sa} is shown for the sake of clarity only. By looking at the capacitor voltages, it is clear that there is a steady increase in V_{c1} , though the amount is very small. Similarly there is a small ,but steady decrease in the capacitor voltage V_{c3}. Hence, even in a loss less system, a voltage control loop is required if $p^{\sim}$ is to be compensated. This voltage control loop is applied to this inverter and discussed as in the subsection that follows.

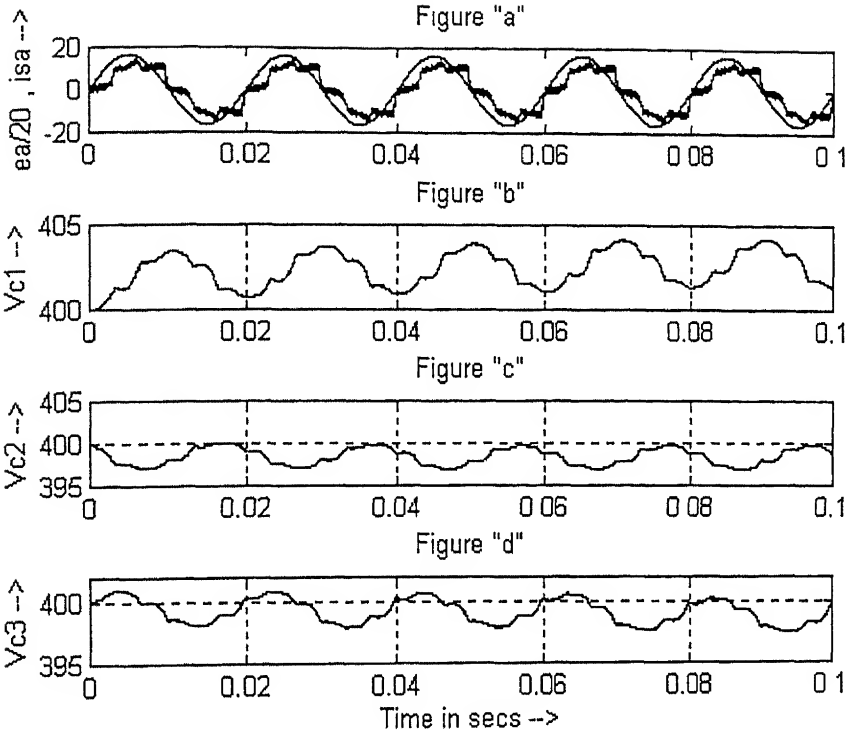

Fig. 5.5 : Capacitor voltages(Over a period of five cycles of input system voltage) when only alternating active power ($\tilde{p}$) is compensated.

5.3.2 Closed-loop Operation

Compensation of the alternating active power component $\tilde{p}$ contributes to the steady deviation of capacitor voltages from the required value. Losses in devices will give rise to further deviation of voltage. Thus, to keep capacitor voltages constant, it is required to modify the value of $\tilde{p}$ that is used for calculating the reference currents as explained in Chapter 2. For clarity (2.4.1) is rewritten as follows.

From (5.3.1), it is clear that the term $p^{\sim}$ should be modified instantaneously to take care of the voltage deviation. The amount by which it should be reduced depends on the voltage errors (the difference between the desired and actual voltages).

$$\begin{bmatrix} i_{c\alpha p\sim}^{*} \\ i_{c\beta p\sim}^{*} \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} * \begin{bmatrix} p^{\sim} \\ 0 \end{bmatrix}. \qquad (5.3.1)$$

This modification is shown in (5.3.2). Where a component p_v representing the total losses is deducted from the term $p^{\sim}$. The corrected power ($p^{\sim} - p_v$), now sets the instantaneous reference currents. These currents flow through the capacitors and tend to make the voltage constant.

$$\begin{bmatrix} i_{c\alpha p\sim}^{*} \\ i_{c\beta p\sim}^{*} \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} * \begin{bmatrix} p^{\sim} - p_v \\ 0 \end{bmatrix}. \qquad (5.3.2)$$

PI controller is used to derive p_v , the amount by which $p^{\sim}$ is to be modified instantaneously [3]. The details of the Compensator system comprising of the control circuits along with the power circuit are shown in Fig. 5.6. The voltage control loop employs PI controller with a gain K_v and time constant T_v as shown in this figure. V_{c1}^{*} is the reference or desired voltage for the capacitor C_1, used for the top inverter. Two such controllers are used for the other two phases and not shown in the figure. Higher values of gain deteriorate the reference currents. Gain K_v and time constant T_v are taken as 2 and 1.5s respectively. All the reference voltages are taken as 400 V. Instantaneous reactive and harmonic power compensation is performed as per the block diagram shown in Fig. 5.6. The results are obtained and then compared with the results in the absence of the control loop. This is explained as follows.

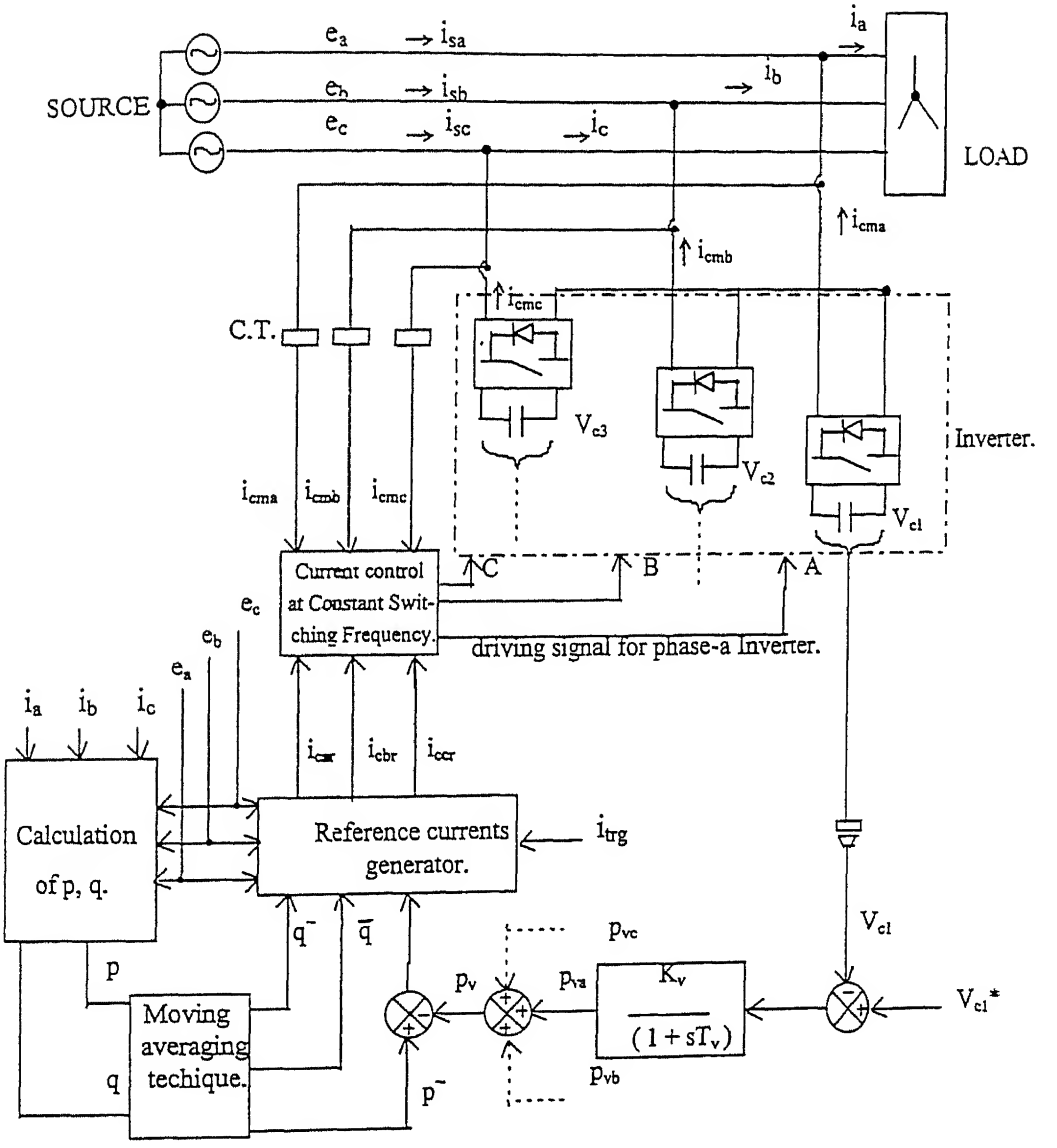

Fig. 5.6 : Block diagram of the three-phase three level Compensator System.

Fig. 5.7 shows the capacitor voltages when the inverter operates without the voltage controller. These voltages are shown for a time interval of seven cycles (0s to 0.14s) of the system voltage. The effect of losses considered is prominent in subfigure c, showing V_{c3} , where the capacitor voltage increase in successive cycles.

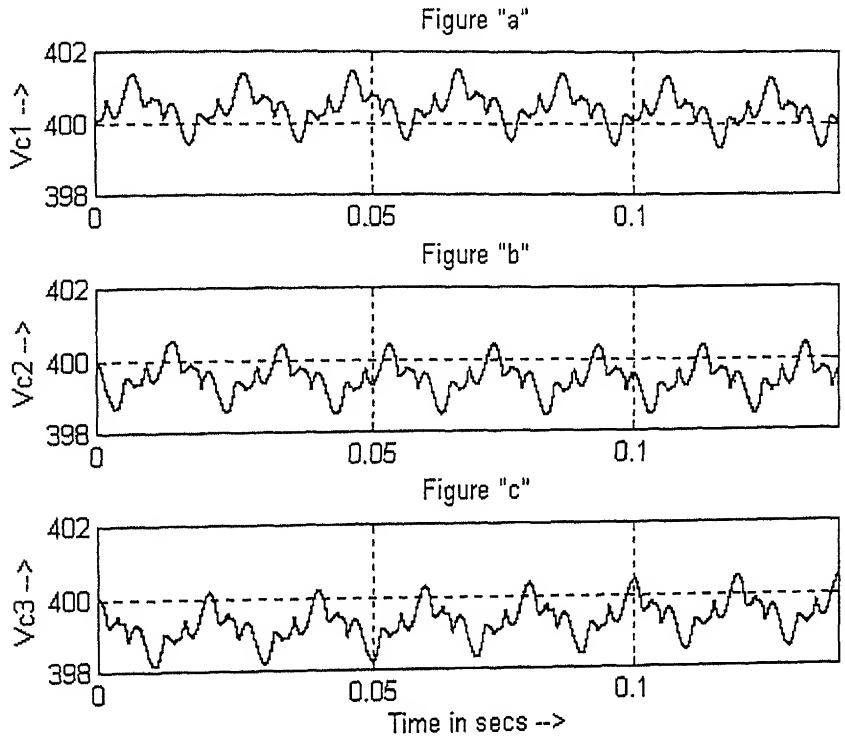

Fig. 5.7 : Capacitor voltages without the presence of voltage control loop.

Compensation is obtained with the presence of the voltage controller to take care of losses. Fig. 5.8 shows the capacitor voltages under this condition. The voltage control makes the capacitor voltages steady in successive cycles as is seen from subfigure c of Fig. 5.8. The steady increase in now not there in V_{c3} of Fig. 5.8. This reveals that the Compensator System as presented in Fig. 5.6 is now suitable for compensation under steady state of a physical system having losses.

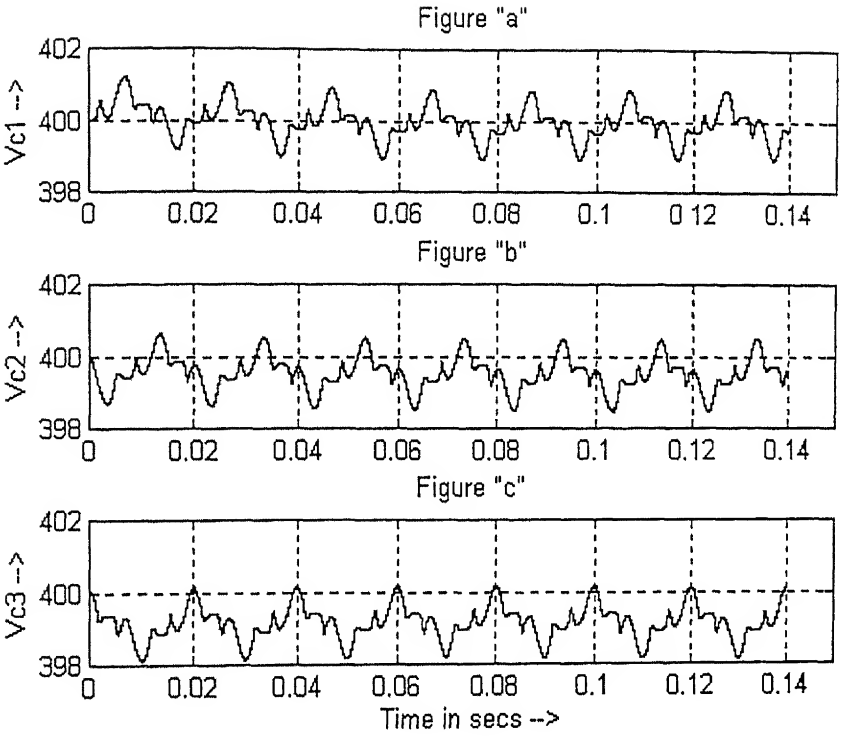

Fig. 5.8 : Capacitor voltages with the presence of voltage control loop.

Fig. 5.9 shows the compensation results when voltage control loop is present in the system. The subfigure a shows the load current i_a. The subfigure b showing E_{an} reveals that the mode of operation for the inverter is selected as described in Sec. 4.3 of Chap. 4 Hence, it is possible to shape the inverter output voltages in any pattern for providing a better current control, without affecting the independent action of the current controller. This is not so in [9], where the three-phase three level NPC inverter is used. Here, the switching conditions for the inverter phases which control the voltages are obtained sacrificing the optimum current control action. The compensated source current i_{sa} of subfigure c reveals that the wave form is superior to that shown in Fig. 4.6 of Chap. 4.

Fig. 5.10 illustrates the compensated source current i_{sa} for one cycle and its harmonics spectrum. This characteristic is almost the same as that for the three-phase three level NPC inverter shown in Fig. 3.19 of Chapter 3.

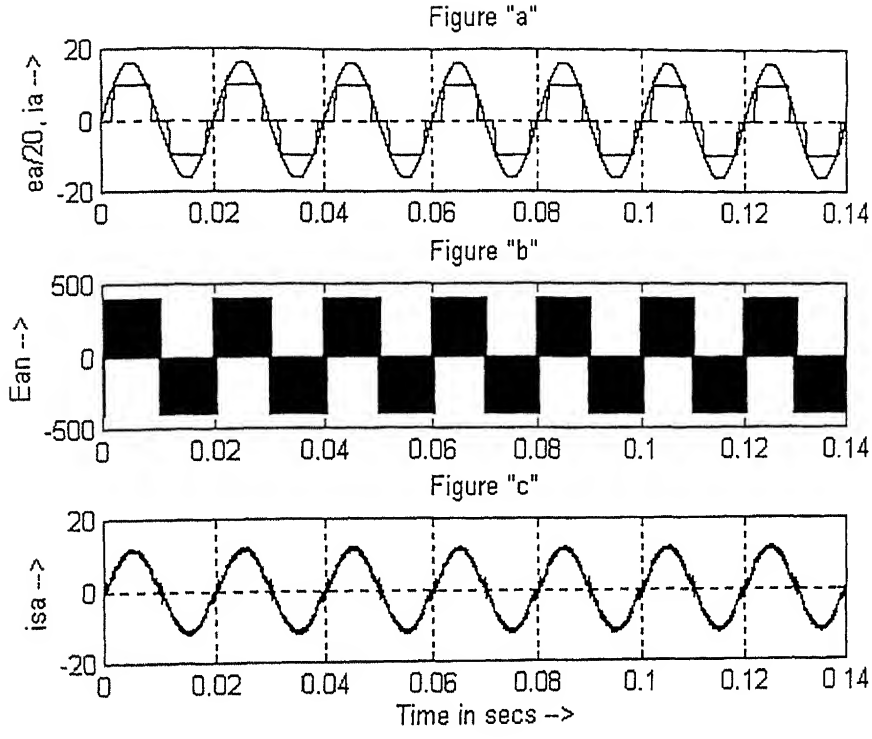

Fig. 5.9 : Compensation results with voltage control loop.

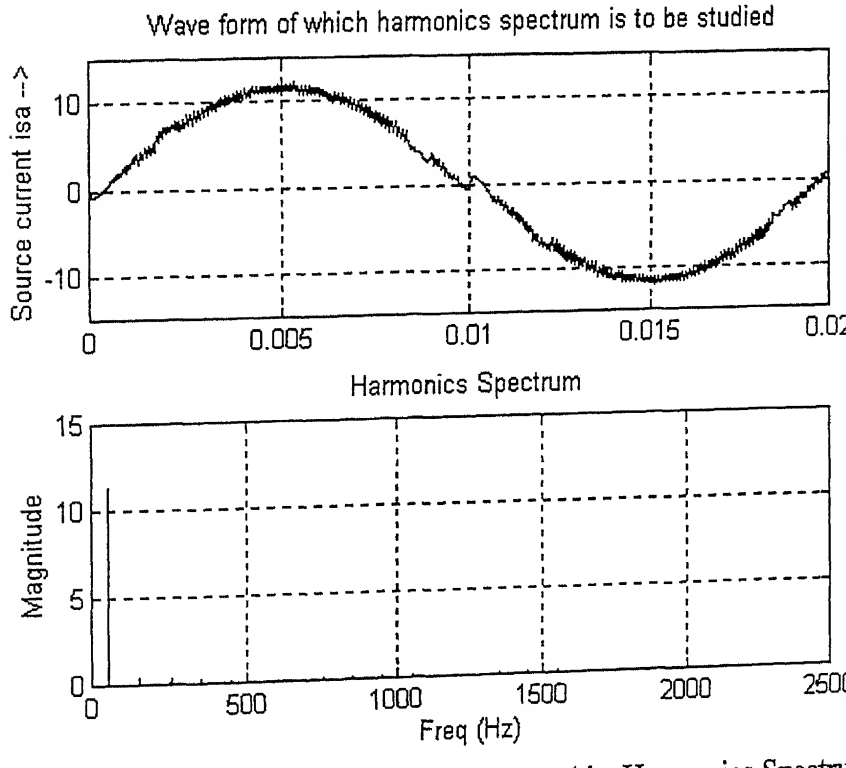

Fig. 5.10 : Compensated Source Current and its Harmonics Spectrum .

Switching signals for three phases (A, B, and C), over a period of half cycle of system voltage are illustrated in Fig. 5.11. This shows that the inverter operates at constant switching frequency.

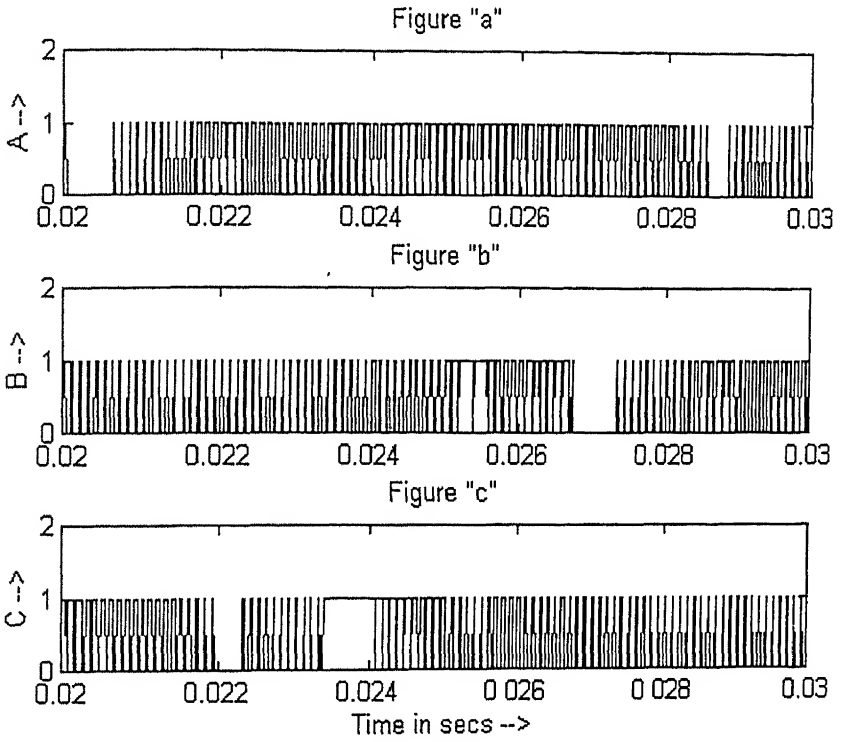

Fig. 5.11 : Switching signals for all the phases, over a half cycle time of system voltage.

5.4 Conclusion

The configuration studied in this chapter is relatively simple. It provides independent current and voltage control for instantaneous reactive and harmonic power compensation as in Fig. 5.6. Any shape of inverter output voltages could be obtained to have better current control without affecting the capacitor voltages. This is not the case with the three level inverter that is described in Chapter 4. It also provides effective compensation characteristics as shown in Fig. 5.10. which reveals that the harmonic components are negligible as compared to the fundamental component of source current. It may also be mentioned that this configuration provides better performance even under unbalanced

conditions as it handles the reference currents independently. The compensator system shown in Fig. 5.6 using this inverter configuration, operates at constant switching frequency. Hence, it possesses all the advantages associated with constant switching frequency operation as described in Chapter 3.

Chapter 6

CONCLUSION

Instantaneous reactive and harmonic power compensation is studied for a controlled rectifier load with two level, three level and five level inverters. The compensation of load reactive and harmonic powers is obtained by using voltage source inverter (VSI) to inject reference currents to the three-phase system. The inverter is operated at constant switching frequency, thereby, exploiting the full potential of switching devices used in the VSI compensator This also reduces the switching losses, stresses on the devices, and size of the compensator system. The constant switching frequency technique is favored for switching devices than the variable frequency offered by Bang-Bang Control. It makes the response faster by allowing to utilize a relatively small value of interfacing inductor between the inverter and the system.

It has been found that the two level inverter fails under unbalanced load conditions. This is the inherent drawback of this configuration of two level inverter.

There is not much difference between the compensation characteristics of three level and five level inverters, though five level inverter provides better compensation. It may not be advisable to use a five level inverter for compensation as it employs more number of devices. In fact it requires twice the number of devices of a three level inverter. The control of compensator is also complicated due to large number of devices.

The three single-phase three level inverter configuration for compensator system presented in this thesis provides better current control capability. The compensator system is relatively simple and provides steady capacitor voltages without increasing the

complexity of the sysetm when compared with that using the three level NPC inverter configuration [9]. The voltage and current control actions being independent of each other makes the compensation better. The shape of output voltages of the inverter is better in this case which makes the system suitable for higher power level. Moreover, as the inverter operates with constant switching frequency technique, the system is relatively compact , provides fast response. Also, the inverter configuration works well even under unbalanced load condtions.

Scope for further work.

The followings are the areas in which further work could be carried out.

1. Practical implementation of the proposed compensator system could be carried out.
2. Fuzzy Logic Controller involving voltage control aspects could be used to select the modes of operation for the Five Level Inverter operating with constant switching frequency for high power applications.
3. Resonant Inverters could be used in the compensator system enabling the system suitable for higher power level.

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